36V Radiation Tolerant Precision Instrumentation Amp with Rail-to-Rail Output Differential ADC Driver

ISL70617SEH

The ISL70617SEH is a high performance, differential input, differential output instrumentation amplifier designed for precision analog-to-digital applications. It can operate over a supply range of 8V (±4V) to 36V (±18V) and features a differential input voltage range up to ±30V. The output stage has rail-to-rail output drive capability optimized for differential ADC driver applications. The output stage is powered by separate supplies. This feature enables the output to be driven by the same low voltage supplies powering the ADC, thereby providing protection from high voltage signals and the low voltage digital circuits. Its versatility makes it suitable for a variety of general purpose applications. Additional features not found in other instrumentation amplifiers enable high levels of DC precision and excellent AC performance.

The gain of the ISL70617SEH can be programmed from 0.1 to 10,000 via two external resistors, R_{IN} and R_{FB}. The gain accuracy is determined by the matching of R_{IN} and R_{FB}. The gain resistors have Kelvin sensing, which removes gain error due to PC trace resistance. The input and output stages have individual power supply pins, which enable input signals riding on a high common-mode voltage to be level shifted to a low voltage device, such as an A/D converter. The rail-to-rail output stage can be powered from the same supplies as the ADC, which preserves the ADC maximum input dynamic range and eliminates ADC input overdrive.

The ISL70617SEH is offered in a 24 Ld ceramic flatpack package with an operating temperature range of -55°C to +125°C.

Features

- Rail-to-rail differential output ADC driver
- Low input offset 30µV
- Input bias current. 0.2nA
- Excellent CMRR and PSRR 120dB
- Wide operating voltage range . . . . . ±4V to ±18V
- Closed loop -3dB BW 0.3MHz (A_V = 1k) to 5.5MHz (A_V = 0.1)
- Operating temperature range. . . . . -55°C to +125°C
- Acceptance tested to 75krad(Si) (LDR) wafer-by-wafer
- Radiation tolerance
  - Low dose rate (0.01rad(Si)/s) . . . . . 75krad(Si)
  - SEB LET_{TH} (V_S = ±18V). . . . . 60MeV•cm^2/mg

Applications

- ADC driver
- Precision test and measurement
- High voltage process control
- Signal conditioning for remote powered sensors
- Satellite communication

Related Literature

- For a full list of related documents, visit our website
  - ISL70617SEH product page

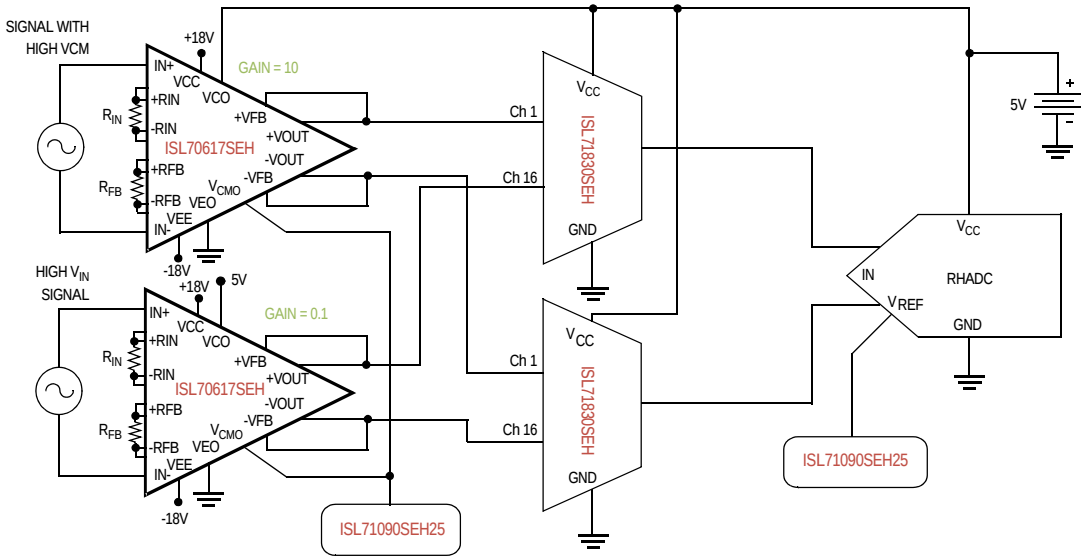


FIGURE 1. COMPLETE SPACE GRADE ANALOG SIGNAL CHAIN

Table of Contents

Ordering Information

SMD/ORDERING NUMBER (Note 1)	PART NUMBER (Note 2)	TEMPERATURE RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
5962L1524602VXC	ISL70617SEHVF	-55 to +125	24 Ld Flatpack	K24.A
N/A	ISL70617SEHF/PROTO	-55 to +125	24 Ld Flatpack	K24.A
5962L1524602V9A	ISL70617SEHVX	-55 to +125	Die	N/A
N/A	ISL70617SEHX/SAMPLE	-55 to +125	Die	N/A
N/A	ISL70617SEHEV1Z	Evaluation Board		

NOTES:

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

TABLE 1. DIFFERENCES BETWEEN FAMILY OF PARTS

SMD/ORDERING NUMBER	PART NUMBER	DIFFERENTIAL INPUT	OUTPUT	GAIN ERROR LOW VOLTAGE	PINOUTS			
					PIN 12	PIN 13	PIN 14	PIN17
5962L1524601VXC	ISL70517SEHVF	Yes	Single-Ended	±0.2	V_{OUT}	NC	V_{REF}	NC
5962L1524602VXC	ISL70617SEHVF	Yes	Differential	±0.1	$+V_{OUT}$	$-V_{OUT}$	$-V_{FB}$	V_{CMO}

Simplified Block Diagram

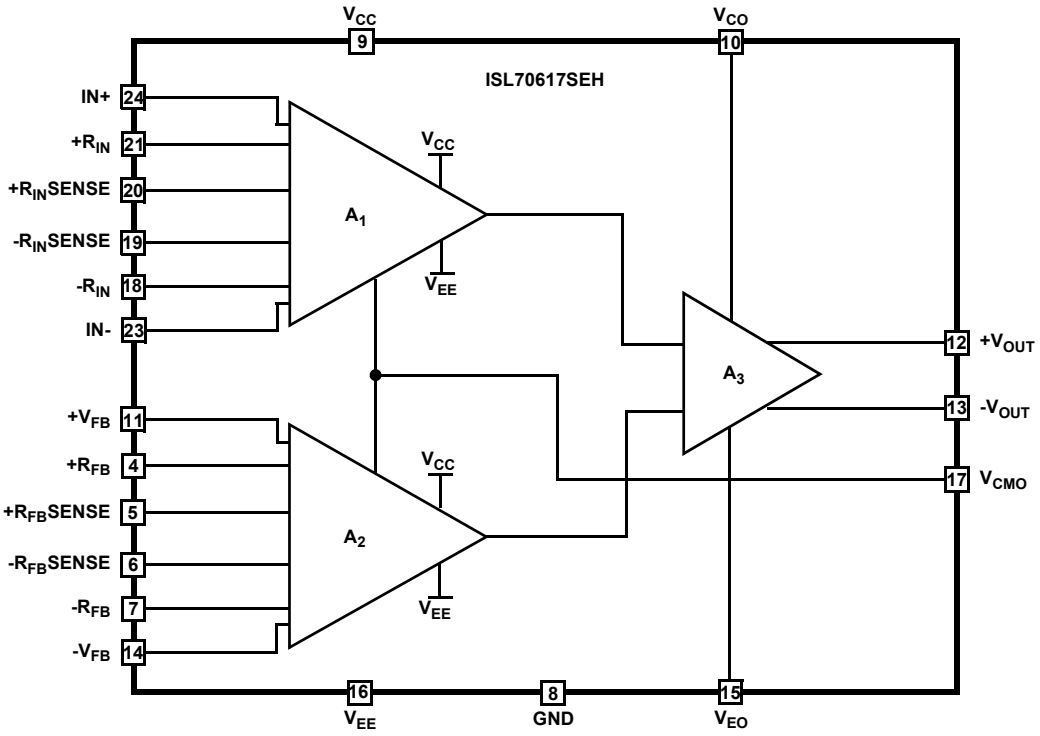
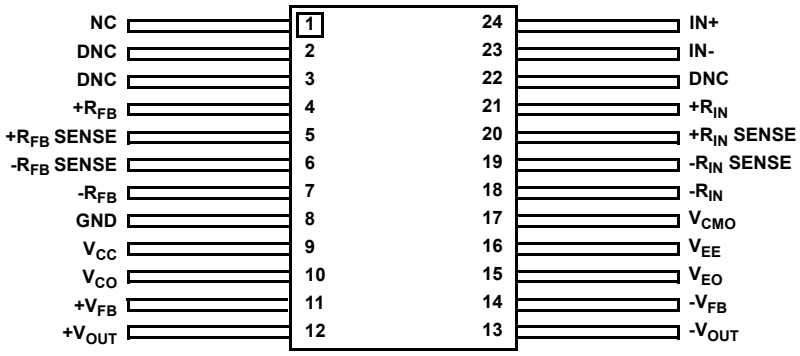


FIGURE 2. SIMPLIFIED BLOCK DIAGRAM

Pin Configuration

ISL70617SEH
(24 LD FLATPACK)
TOP VIEW



NOTE: The small square mark is indicative of pin #1.

Pin Descriptions

PIN NAME	PIN NUMBERS	DESCRIPTION
NC	1	No internal connection
DNC	2, 3, 22	For internal use. Do not connect
$+R_{FB}$	4	Feedback resistor R_{FB}, positive terminal
$+R_{FB}$ SENSE	5	$+R_{FB}$ positive sense pin connects to the resistor R_{FB}+ terminal to form the R_{FB}+ Kelvin connection.
$-R_{FB}$ SENSE	6	$-R_{FB}$ negative sense pin connects to the resistor R_{FB}- terminal to form the R_{FB}- Kelvin connection.
$-R_{FB}$	7	Feedback resistor R_{FB}, negative terminal
GND	8	Ground pin is capacitively coupled to the internal ESD circuit and should be connected to power supply common or signal GND. Also connected to the lid.
V_{CC}	9	Positive supply for input stage and feedback amplifier
V_{CO}	10	Positive supply for output stage
$+V_{FB}$	11	Positive output feedback
$+V_{OUT}$	12	Positive output
$-V_{OUT}$	13	Negative output
$-V_{FB}$	14	Negative output feedback
V_{EO}	15	Negative supply for output stage
V_{EE}	16	Negative supply for input stage and feedback amplifier
V_{CMO}	17	Output common-mode reference input
$-R_{IN}$	18	Input resistor R_{IN}, negative terminal
$-R_{IN}$ SENSE	19	$-R_{IN}$ negative sense pin connects to the resistor R_{IN}- terminal to form the R_{IN}- Kelvin connection.
$+R_{IN}$ SENSE	20	$+R_{IN}$ positive sense pin connects to the resistor R_{IN}+ terminal to form the R_{IN}+ Kelvin connection.
$+R_{IN}$	21	Input resistor R_{IN}, positive terminal
IN-	23	Negative input
IN+	24	Positive input
LID	N/A	Package lid is internally connected to GND (Pin 8).

Absolute Maximum Ratings

Maximum Supply Voltage (V_{CC} to V_{EE} or GND) 42V
Maximum Supply Voltage (V_{CO} to V_{EO} or GND) 42V
Maximum Voltage (V_{CO} to V_{CC}) . . . . . +0.5V, -40V
Maximum Voltage (V_{EO} to V-) . . . . . -0.5V, +40V
Maximum Differential Input Current . . . . . ±10mA
Max/Min Input Current for Input Voltage >V_{CC} or <V_{EE} . . . . . ±10mA
Maximum Input Current (±R_{IN}, ±R_{FB}, ±R_{IN}SENSE, ±R_{FB}SENSE) . . . ±5mA
Maximum Differential Input Voltage 40V
Min/Max Input Voltage . . . . . (V_{EE} - 0.5V) to (V_{CC} +0.5V)
Output Short-Circuit Duration (1 Output at a Time) . . . . . Continuous
ESD Rating
Human Body Model (Tested per MIL-STD-883 TM 3015) 6kV
Machine Model (Tested per JESD22-A115-C) 250V
Charged Device Model (Tested per JS-002-2014) 1kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld CFP (Notes 3, 4)	60	7

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . . +150°C

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . . -55°C to +125°C
V_{CC}, V_{EE} Operating Voltage Range . . . . . ±4V to ±18V
V_{CO}, V_{EO} Operating Voltage Range . . . . . ±1.5V to ±18V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the "case temp" location is the center of the ceramic on the package underside.

Electrical Specifications

V_{CC} = V_{CO} = 18V, V_{EE} = V_{EO} = -18V, V_{CM} = 0V, R_L = 10kΩ, R_{FB} = R_{IN} = 30.1kΩ, T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C and across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s, unless otherwise specified.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
INPUT DC SPECIFICATIONS						
V_{CMIR}IN	IN+, IN- Common-Mode Input Voltage Range	Verified via CMRR	**V_{EE} + 3V**		**V_{CC} - 3V**	V
V_{OS}IN	Input Offset Voltage	(Notes 10, 11)	-100	±30	100	µV
			-300		**300**	µV
TCV_{OS}IN	Input Offset Voltage Temperature Coefficient		**-4.0**	±0.3	**4.0**	µV/°C
I_BIN	Input Bias Current	(Note 12)	-2.0	±0.2	2.0	nA
			-25		**25**	nA
I_{OS}IN	Input Offset Current	(Note 12)	-1.5	±0.2	1.5	nA
			-18.5		**18.5**	nA
I_{RIN}	Input Resistor Drive Current (Current through R_{IN} resistor)	(Note 9)	87	102	117	µA
R_{IN}CM	Common-Mode Input Resistance	(Note 9)		80		GΩ
CMRR	Common-Mode Rejection Ratio V_{CC} = V_{CO} = 15V, V_{EE} = V_{EO} = -15V Reference Figures 38 and 39	V_{EE} +3V ≤ V_{CM} ≤ V_{CC} -3V G = 1 (Note 15)	110	120		dB
			97			dB
		V_{EE} +3V ≤ V_{CM} ≤ V_{CC} -3V G = 100 (Note 15)	120	150		dB
			120			dB
FEEDBACK DC SPECIFICATIONS						
V_{CMIR}FB	+FB, -FB Common-Mode Input Voltage Range	Verified via CMRR	**V_{EE} + 3V**		**V_{CC} - 3V**	V
V_{OS}FB	Feedback Input Offset Voltage	(Notes 10, 11) +25°C	-1600	±400	1600	µV
		(Notes 10, 11) -55°C to +125°C	-3000		3000	µV
		(Notes 10, 11) +25°C post 75krad	**-6000**		**6000**	µV
TCV_{OS}FB	Feedback Input Voltage Temperature Coefficient		**15.0**	±2.6	**15.0**	µV/°C

Electrical Specifications $V_{CC} = V_{CO} = 18V$, $V_{EE} = V_{EO} = -18V$, $V_{CM} = 0V$, $R_L = 10k\Omega$, $R_{FB} = R_{IN} = 30.1k\Omega$, $T_A = +25°C$, unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C and across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s, unless otherwise specified. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
I_BV_{FB}	Input Bias Current at V_{FB} ± Inputs	(Notes 8, 10, 11)	**-200**	15	**200**	nA
I_{RFB}	Feedback Resistor Drive Current (Current through R_{FB} resistor)	(Note 9)	87	102	117	µA
OUTPUT DC SPECIFICATIONS						
V_{OL}	Output Voltage Low, V_{OUT} to V_{EO}	V_{CC} = +18V, V_{EE} = -18V, V_{CO} = +4V, V_{EO} = -4V, $R_{IN} = R_F$ = 121kΩ, I_{OUT} = 0mA (Note 13)		100	160	mV
					160	mV
		V_{CC} = +18V, V_{EE} = -18V, V_{CO} = +4V, V_{EO} = -4V, $R_{IN} = R_F$ = 121kΩ, I_{OUT} = 1.5mA		150	200	mV
					200	mV
		V_{CC} = +18V, V_{EE} = -18V, V_{CO} = +4V, V_{EO} = -4V, $R_{IN} = R_F$ = 121kΩ, I_{OUT} = 7.5mA		450	550	mV
					550	mV
V_{OH}	Output Voltage High, V_{OUT} to V_{CO}	V_{CC} = +18V, V_{EE} = -18V, V_{CO} = +4V, V_{EO} = -4V, $R_{IN} = R_F$ = 121kΩ, I_{OUT} = 0mA (Note 13)	-160	-100		mV
			-160			mV
		V_{CC} = +18V, V_{EE} = -18V, V_{CO} = +4V, V_{EO} = -4V, $R_{IN} = R_F$ = 121kΩ, I_{OUT} = -1.5mA	-200	-150		mV
			-200			mV
		V_{CC} = +18V, V_{EE} = -18V, V_{CO} = +4V, V_{EO} = -4V, $R_{IN} = R_F$ = 121kΩ, I_{OUT} = -7.5mA	-550	-450		mV
			-550			mV
$V_{OL}LV$	Output Voltage Low, V_{OUT} to V_{EO}	V_{CC} = +4V, V_{EE} = -4V, V_{CO} = +1.5V, V_{EO} = -1.5V, $R_{IN} = R_F$ = 121kΩ, I_{OUT} = 1.5mA		150	200	mV
					200	mV
$V_{OH}LV$	Output Voltage High, V_{OUT} to V_{CO}	V_{CC} = +4V, V_{EE} = -4V, V_{CO} = +1.5V, V_{EO} = -1.5V, $R_{IN} = R_F$ = 121kΩ, I_{OUT} = 1.5mA	-200	-150		mV
			-200			mV
I_{SC}	Output Short-Circuit Current	Output Sink Current V_{OUT} = GND (Note 12)	**20**	45		mA
		Output Source Current V_{OUT} = GND (Note 12)	**20**	45		mA
E_G	Gain Error	V_{OUT} = ±10V, R_F = 121kΩ, G = 1 (Notes 6, 7, 13)	**-0.020**	-0.005	**0.020**	%
		V_{OUT} = ±10V, R_F = 121kΩ, G = 100 (Notes 6, 7, 13)	**-0.045**	-0.020	**0.045**	%
		V_{OUT} = ±2.5V, R_F = 30.1kΩ, G = 1 (Notes 6, 7, 13)	**-0.040**	0.006	**0.040**	%

Electrical Specifications

V_{CC} = V_{CO} = 18V, V_{EE} = V_{EO} = -18V, V_{CM} = 0V, R_L = 10kΩ, R_{FB} = R_{IN} = 30.1kΩ, T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C and across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s, unless otherwise specified. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
$E_{G\ LV}$	Gain Error	V_{CC} = +4V, V_{EE} = -4V, V_{CO} = +1.5V, V_{EO} = -1.5V V_{OUT} = ±0.1V, R_F = 121kΩ G = 1 (Notes 6, 7)	**-0.100**	±0.003	**0.100**	%
		V_{CC} = +4V, V_{EE} = -4V, V_{CO} = +1.5V, V_{EO} = -1.5V V_{OUT} = ±1.25V, R_F = 121kΩ G = 100 (Notes 6, 7)	**-0.100**	±0.004	**0.100**	%
		V_{CC} = +4V, V_{EE} = -4V, V_{CO} = +1.5V, V_{EO} = -1.5V V_{OUT} = -0.1V to +0.1V, R_F = 30.1kΩ G = 1 (Notes 6, 7)	**-0.1000**	±0.0005	**0.1000**	%
V_{OS}OUT	Output Offset Voltage	R_F = 30.1kΩ, (Notes 10, 11)	-10.0	±0.5	10.0	mV
		R_F = 121kΩ, (Notes 10, 11)	**-40**		**40**	mV
OUTPUT COMMON-MODE SPECIFICATIONS						
V_{CMO}CMIR	Output Common-Mode Control Input Voltage Range	Verified by V_{OS}CM and I_BV_{CMO}	**V_{EE} + 3V**		**V_{CC} - 3V**	V
V_{OS}CM	Output Common-Mode Offset Voltage from V_{CMO} Input	(Note 12)	-1.3	±0.5	1.3	mV
			-6.0		**6.0**	mV
I_BV_{CMO}	Input Bias Current at V_{CMO} Input	(Note 12)	**-600**	±200	**600**	nA
POWER SUPPLY SPECIFICATIONS						
I_{CC}	Input Stage Supply Current	R_L = 10k, IN+ = IN- = 0V (Note 10)		2.05	2.40	mA
					3.0	mA
I_{EE}	Input Stage Supply Current	R_L = 10k, IN+ = IN- = 0V (Note 10)	-2.40	-2.05		mA
			-3.00			mA
I_{CO}	Output Stage Supply Current	R_L = 10k, IN+ = IN- = 0V (Note 10)		2.25	2.60	mA
					3.0	mA
I_{EO}	Output Stage Supply Current	R_L = 10k, IN+ = IN- = 0V (Note 10)	-2.60	-2.25		mA
			-3.0			mA
V_{CC} to V_{EE}	Input Supply Voltage		**±4**		**±18**	V
V_{CO} to V_{EO}	Output Supply Voltage		**±1.5**		**±18**	V
PSRR V_{CC} to V_{EE}	Input Power Supply Rejection Ratio	V_{CC} to V_{EE} = ±4V to ±18V	123	130		dB
		(Note 15)	**110**			dB
PSRR V_{CO} to V_{EO}	Output Power Supply Rejection Ratio	V_{CO} to V_{EO} = ±1.5V to ±18V (Note 15)	110	120		dB
			90			dB
AC SPECIFICATIONS						
$e_{N(RTO)}$	Total Noise Voltage Noise Density Referred to Output	f = 1kHz, (Note 14)		86		nV/√Hz
e_N(I)	Input Noise Voltage Density	f = 1kHz, (Note 14)		8.6		nV/√Hz
e_N(FB)	Feedback Noise Voltage Density	f = 1kHz, (Note 14)		8.6		nV/√Hz
e_N V_{P-P}	Input V_{P-P} Noise Voltage	f = 0.1Hz to 10Hz		5.7		μV_{P-P}
i_N(I)	Input Noise Current Density	f = 1kHz, (Note 14)		150		fA/√Hz

Electrical Specifications $V_{CC} = V_{CO} = 18V$, $V_{EE} = V_{EO} = -18V$, $V_{CM} = 0V$, $R_L = 10k\Omega$, $R_{FB} = R_{IN} = 30.1k\Omega$, $T_A = +25°C$, unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C and across a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s, unless otherwise specified. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
i_N(IERR)	Total Internal Noise Current Density	f = 1kHz, (Note 14)		2.6		pA/√Hz
i_NIERR RMS	0.1Hz to 10Hz Total Internal RMS Noise Current	f = 0.1Hz to 10Hz		4		pA_{RMS}
-3dB BW	-3dB Bandwidth vs Closed Loop Gain, R_{FB} = 30.1k	R_{FB} = 30.1kΩ; R_{IN} = 301kΩ; G = 0.1		5.5		MHz
		R_{FB} = 30.1kΩ; R_{IN} = 30.1kΩ; G = 1		2.6		MHz
		R_{FB} = 30.1kΩ; R_{IN} = 3.01kΩ; G = 10		2.2		MHz
		R_{FB} = 30.1kΩ; R_{IN} = 301Ω; G = 100		2.0		MHz
		R_{FB} = 30.1kΩ; R_{IN} = 30.1Ω; G = 1000		0.3		MHz
-3dB BW	-3dB Bandwidth vs Closed Loop Gain, R_{FB} = 121k	R_{FB} = 121kΩ; R_{IN} = 1.21MΩ; G = 0.1		5.0		MHz
		R_{FB} = 121kΩ; R_{IN} = 121kΩ; G = 1		1.4		MHz
		R_{FB} = 121kΩ; R_{IN} = 12.1kΩ; G = 10		0.5		MHz
		R_{FB} = 121kΩ; R_{IN} = 1.21kΩ; G = 100		0.45		MHz
		R_{FB} = 121kΩ; R_{IN} = 121Ω; G = 1000		0.4		MHz
SR	Slew Rate			4		V/µs
t_S	Settling Time to 0.01%	V_{OUT} = ±2.4V, R_F = 30.1kΩ		3		µs
		V_{OUT} = ±9.6V, R_F = 121kΩ		11		µs

NOTES:

5. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
6. Differential gain (A_V) = R_{FB}/R_{IN}.
7. $\pm V_{OUT}$, clipping ~ $I_{RF}*R_{FB}$.
8. $I_BV_{FB} = (V_{OS}OUT - (R_{FB}/R_{IN})*V_{OS}IN - V_{OS}FB)/R_{FB}$.
9. Compliance to datasheet limits is assured by design simulation.
10. V_{CC}, V_{CO} = 4V, 5V, 15V, 18V, V_{EE}, V_{EO} = -4V, -5V, -15V, -18V.
11. V_{CC} = 18V, V_{EE} = -18V, V_{CO} = 1.5V, V_{EO} = -1.5V.
12. V_{CC}, V_{CO} = 5V, 18V, V_{EE}, V_{EO} = -5V, -18V.
13. V_{CC}, V_{CO} = 18V, 21V, V_{EE}, V_{EO} = -18V, -21V.
14. Total noise calculated with Equation 17 on page 22.
15. Rejection ratio numbers are reported as absolute values.

Typical Post Radiation Performance Curves

$V_{CC} = V_{CO} = 18V, V_{EE} = V_{EO} = -18V, V_{CM} = 0V, R_L = Open$, unless otherwise specified. Error bars (if shown) are based on minimum and maximum data.

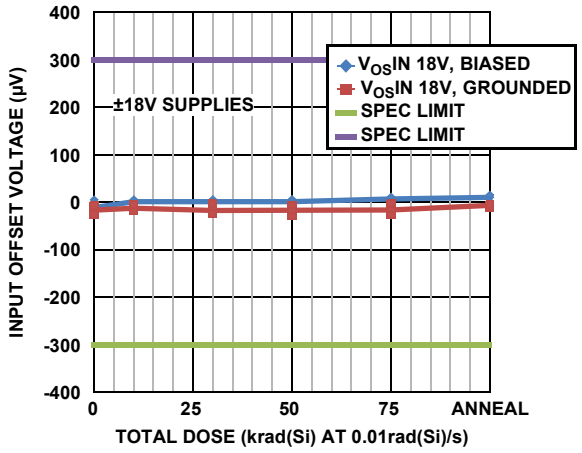


FIGURE 3. INPUT OFFSET VOLTAGE vs TOTAL DOSE

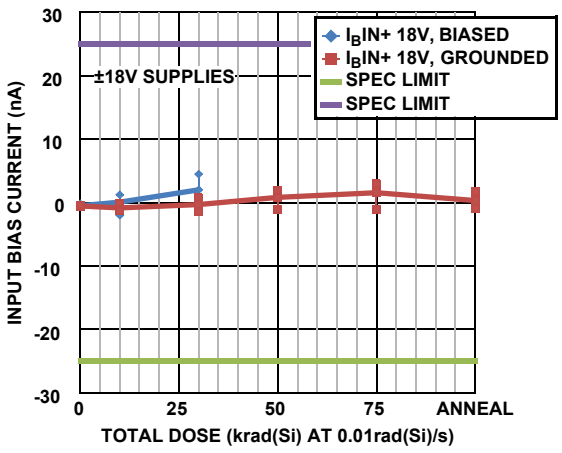


FIGURE 4. INPUT BIAS CURRENT I_BIN+ vs TOTAL DOSE

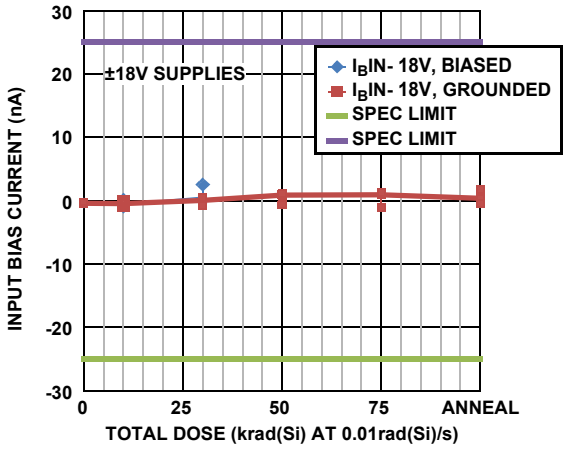


FIGURE 5. INPUT BIAS CURRENT I_BIN- vs TOTAL DOSE

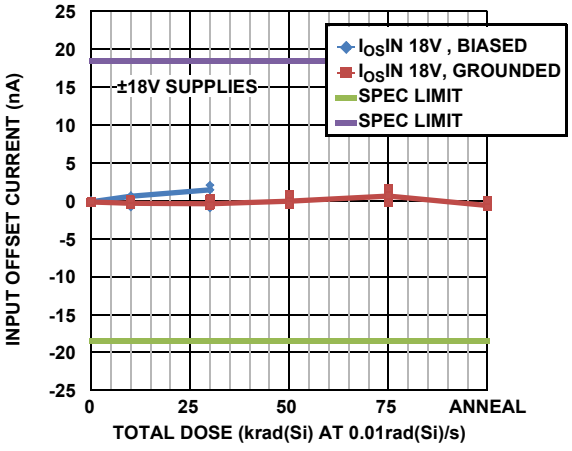


FIGURE 6. INPUT OFFSET CURRENT vs TOTAL DOSE

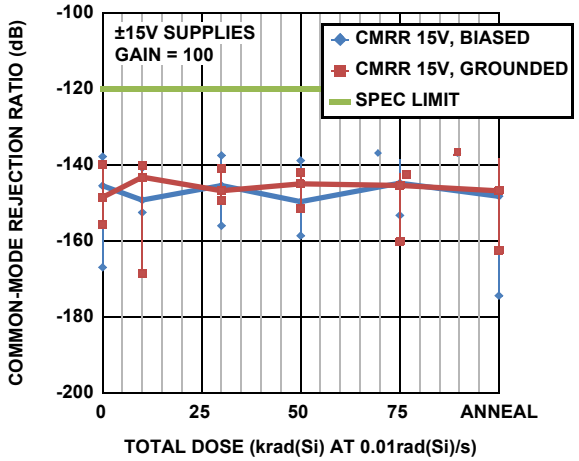


FIGURE 7. CMRR (RTI), GAIN = 100 vs TOTAL DOSE

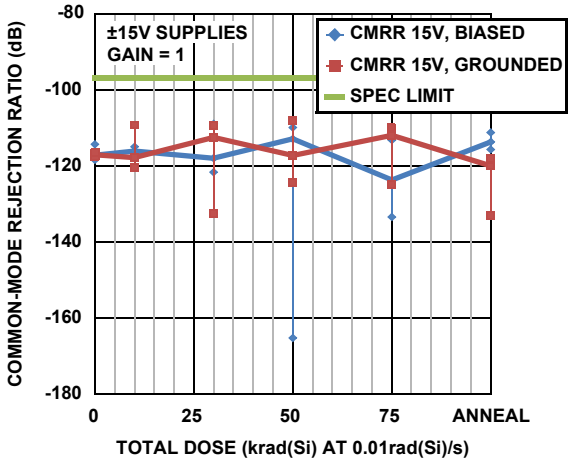


FIGURE 8. CMRR (RTI), GAIN = 1 vs TOTAL DOSE

Typical Post Radiation Performance Curves

$V_{CC} = V_{CO} = 18V$, $V_{EE} = V_{EO} = -18V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. Error bars (if shown) are based on minimum and maximum data. **(Continued)**

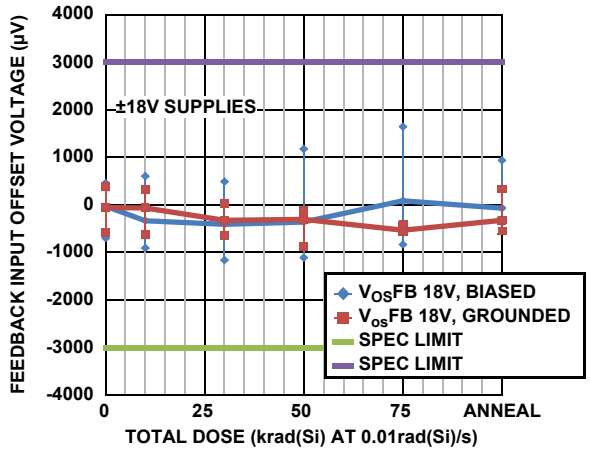


FIGURE 9. $V_{OS}FB$ vs TOTAL DOSE

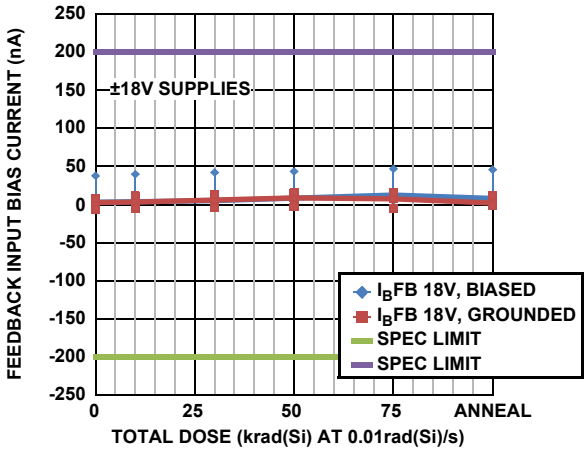


FIGURE 10. $I_B FB$ vs TOTAL DOSE

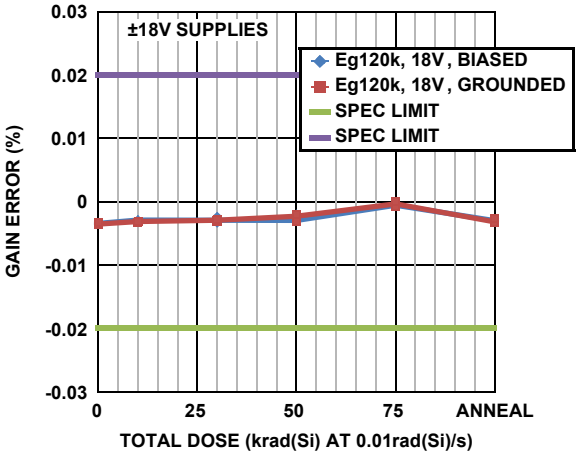


FIGURE 11. GAIN ERROR (GAIN = 1) vs TOTAL DOSE

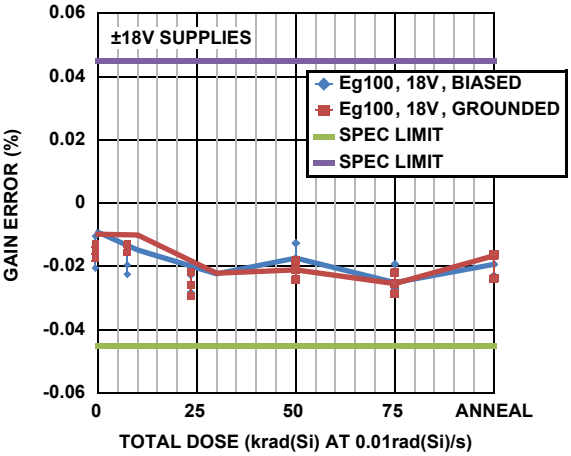


FIGURE 12. GAIN ERROR (GAIN = 100) vs TOTAL DOSE

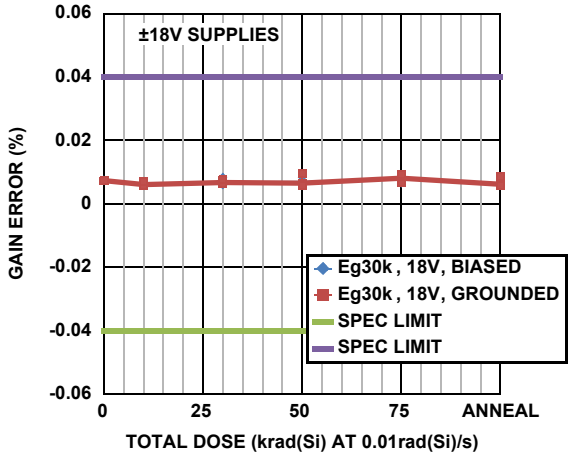


FIGURE 13. GAIN ERROR (GAIN = 1) vs TOTAL DOSE

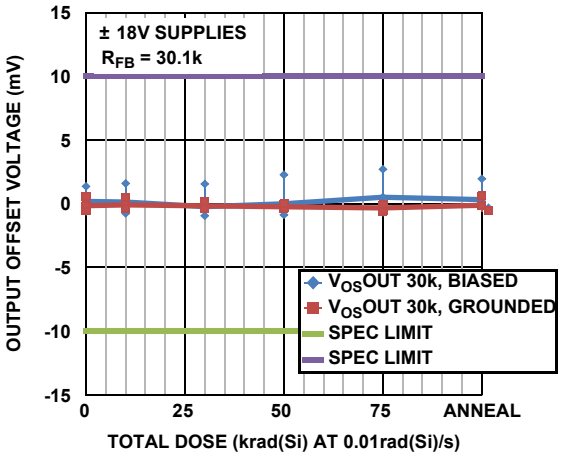


FIGURE 14. $V_{OS}OUT$ (GAIN = 1) vs TOTAL DOSE

Typical Post Radiation Performance Curves

$V_{CC} = V_{CO} = 18V$, $V_{EE} = V_{EO} = -18V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. Error bars (if shown) are based on minimum and maximum data. **(Continued)**

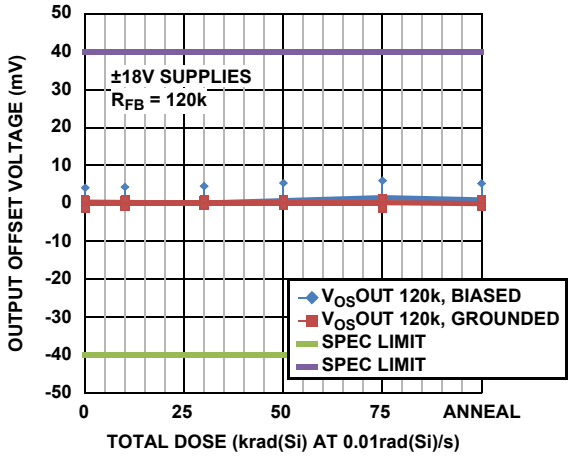


FIGURE 15. V_{OS}OUT (Gain = 1) vs TOTAL DOSE

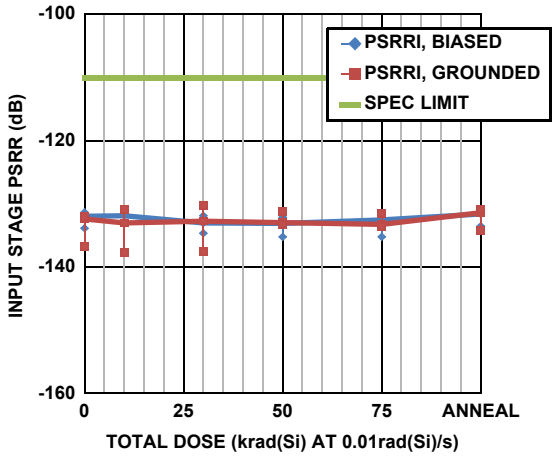


FIGURE 16. INPUT STAGE PSRR vs TOTAL DOSE

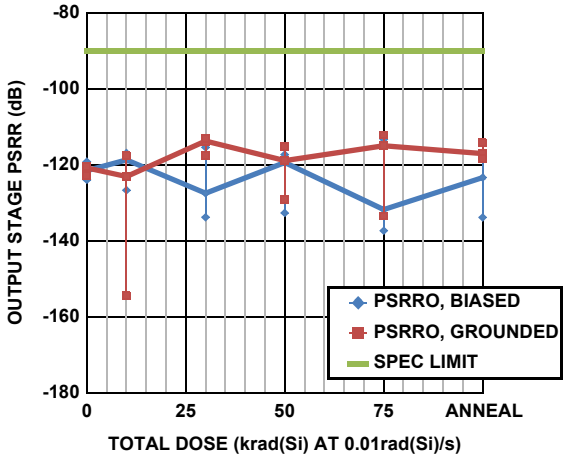


FIGURE 17. OUTPUT STAGE PSRR vs TOTAL DOSE

Typical Performance Curves

$V_{CC} = V_{CO} = 18V$, $V_{EE} = V_{EO} = -18V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified.

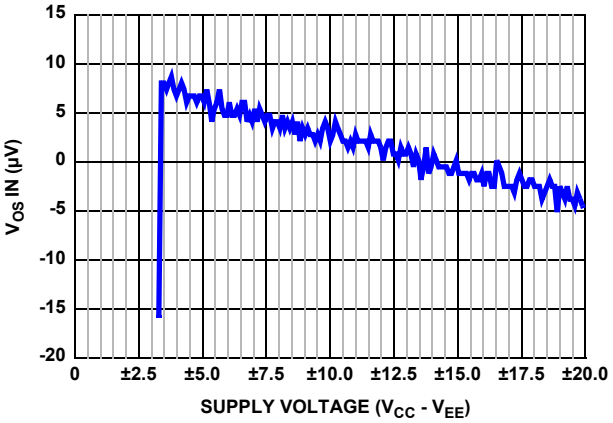


FIGURE 18. $V_{OS}IN$ vs SUPPLY VOLTAGE

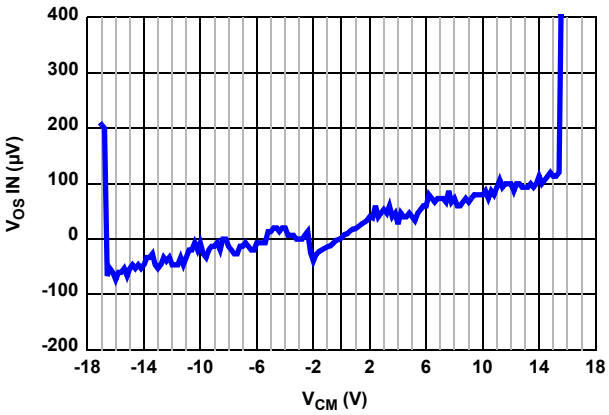


FIGURE 19. $V_{OS}IN$ vs INPUT COMMON MODE VOLTAGE

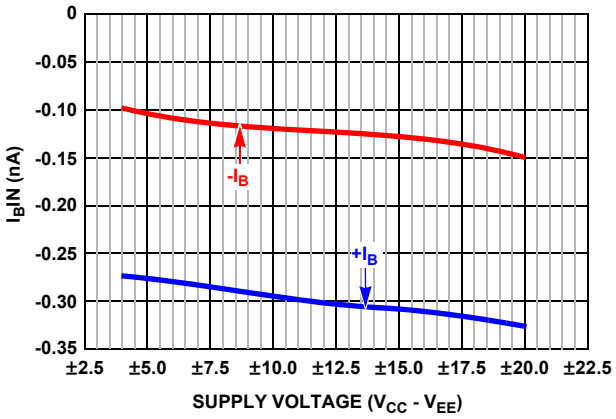


FIGURE 20. I_BIN vs SUPPLY VOLTAGE

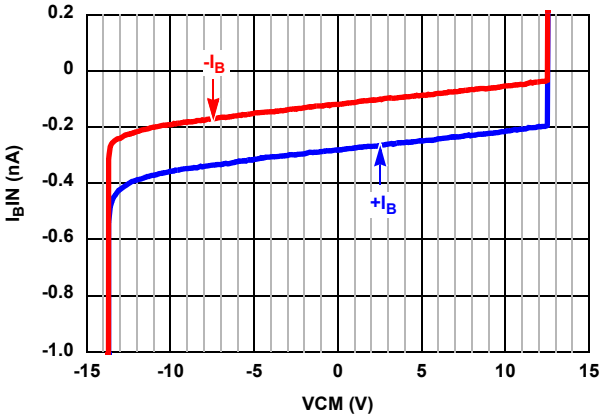


FIGURE 21. I_BIN vs INPUT COMMON-MODE VOLTAGE (±15V)

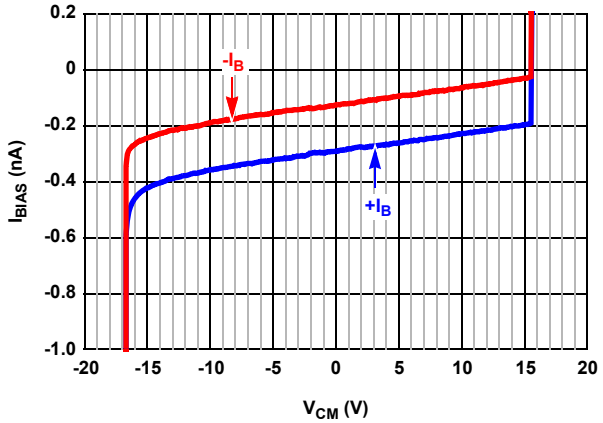


FIGURE 22. I_B vs INPUT COMMON-MODE VOLTAGE (±18V)

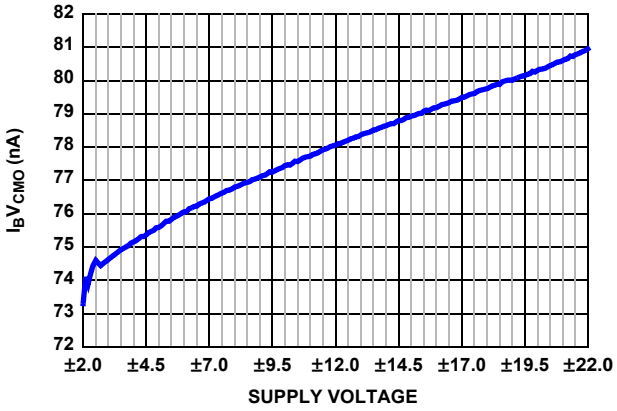


FIGURE 23. I_BV_{CMO} vs SUPPLY VOLTAGE ($V_{CC} - V_{EE}$)

Typical Performance Curves

$V_{CC} = V_{CO} = 18V$, $V_{EE} = V_{EO} = -18V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

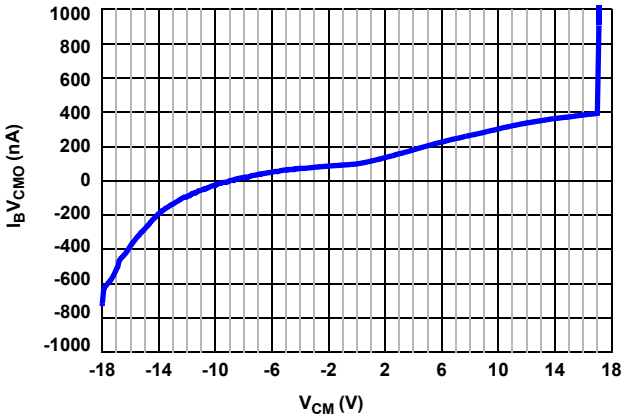


FIGURE 24. I_BV_{CMO} vs INPUT COMMON-MODE VOLTAGE

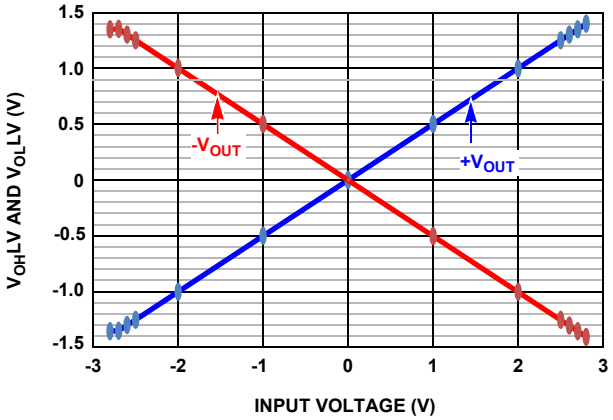


FIGURE 25. V_{OH} AND V_{OL}

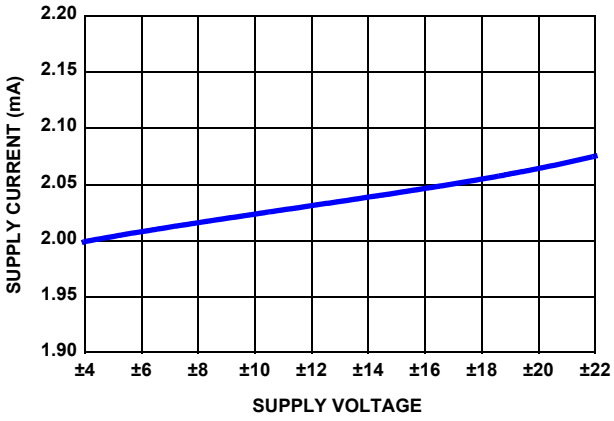


FIGURE 26. I_{CC} vs SUPPLY VOLTAGE (V_{CC} - V_{EE})

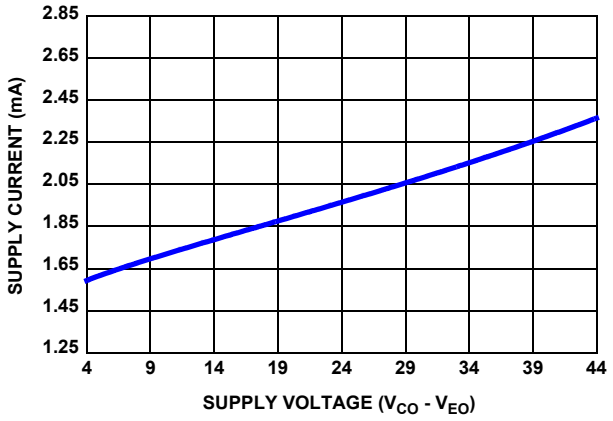


FIGURE 27. I_{CO} vs SUPPLY VOLTAGE (V_{CO} - V_{EO})

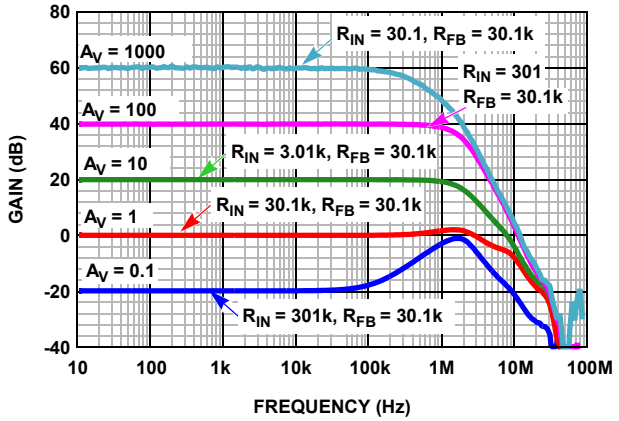


FIGURE 28. CLOSED LOOP GAIN (R_{FB} = 30.1k) vs FREQUENCY

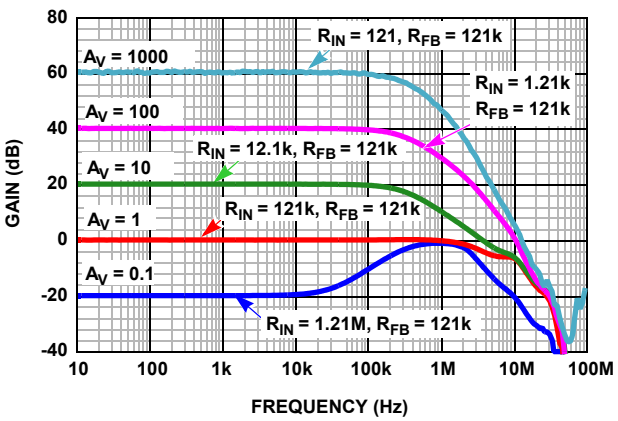


FIGURE 29. CLOSED LOOP GAIN (R_{FB} = 121k) vs FREQUENCY

Typical Performance Curves

$V_{CC} = V_{CO} = 18V$, $V_{EE} = V_{EO} = -18V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

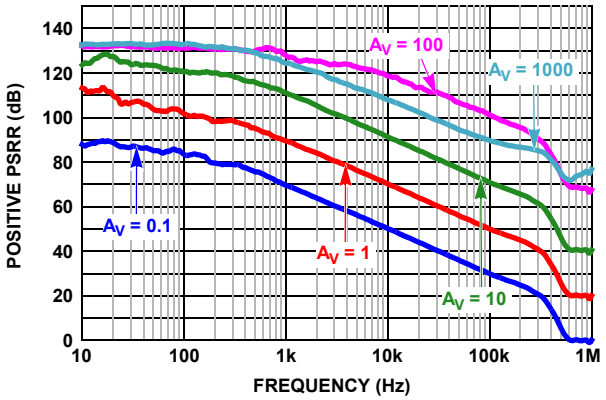


FIGURE 30. POSITIVE PSRR V_{CC} SUPPLY RTI (R_F = 30.1k)

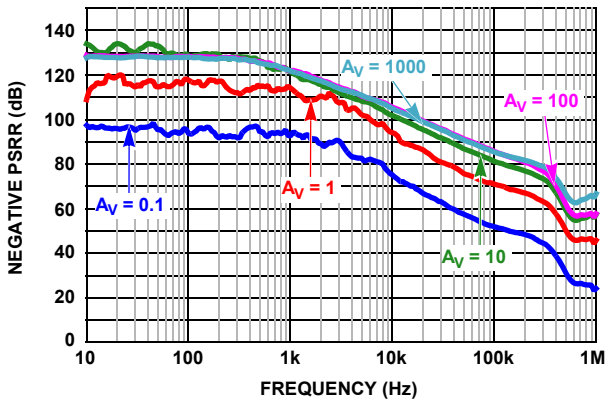


FIGURE 31. NEGATIVE PSRR V_{EE} SUPPLY RTI (R_F = 30.1k)

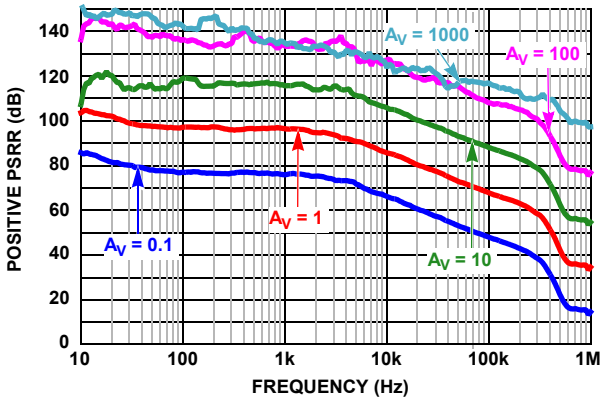


FIGURE 32. POSITIVE PSRR V_{CO} SUPPLY RTI (R_F = 30.1k)

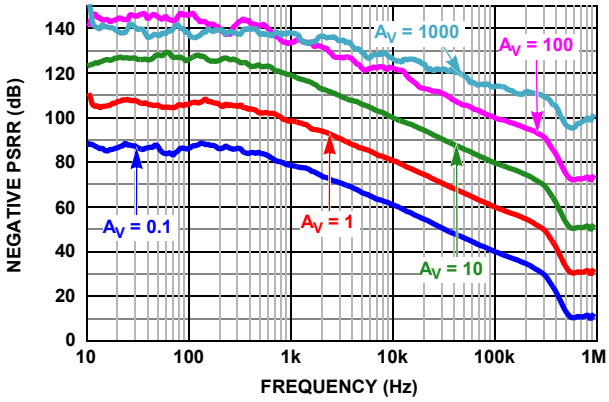


FIGURE 33. NEGATIVE PSRR V_{EO} SUPPLY RTI (R_F = 30.1k)

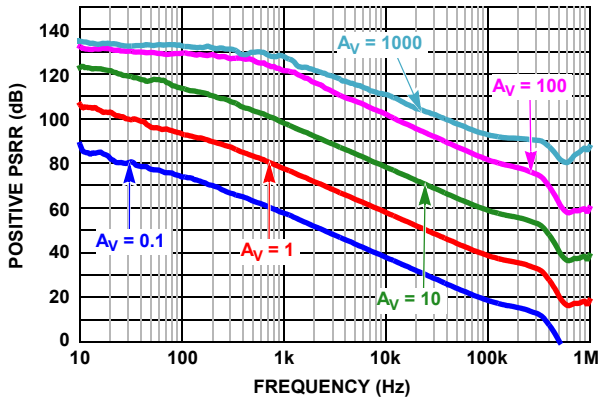


FIGURE 34. POSITIVE PSRR V_{CC} SUPPLY RTI (R_F = 121k)

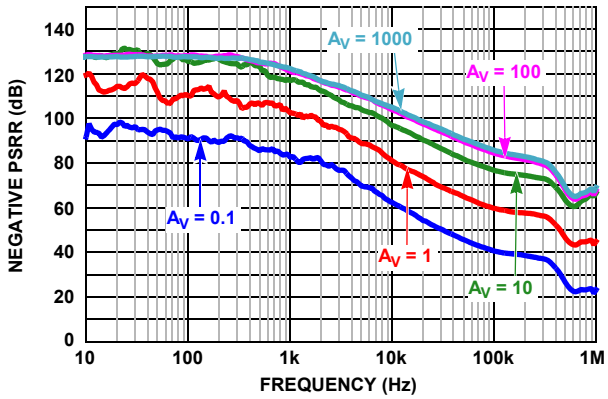


FIGURE 35. NEGATIVE PSRR V_{EE} SUPPLY RTI (R_F = 121k)

Typical Performance Curves

$V_{CC} = V_{CO} = 18V$, $V_{EE} = V_{EO} = -18V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

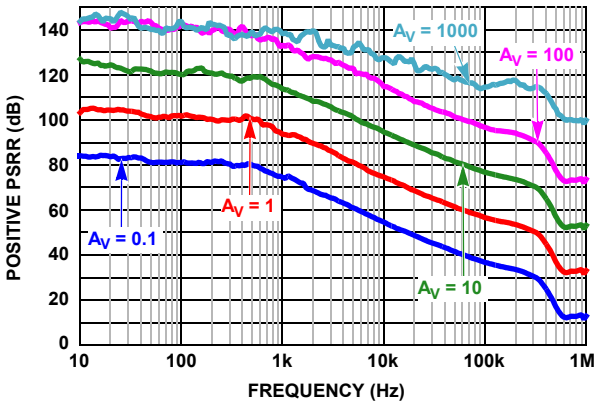


FIGURE 36. POSITIVE PSRR V_{CO} SUPPLY RTI (R_F = 121k)

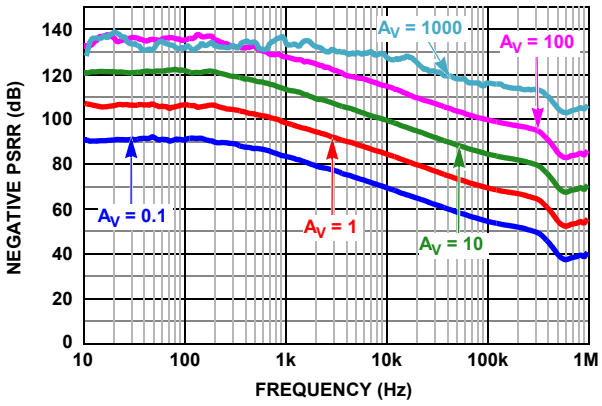


FIGURE 37. NEGATIVE PSRR V_{EO} SUPPLY RTI (R_F = 121k)

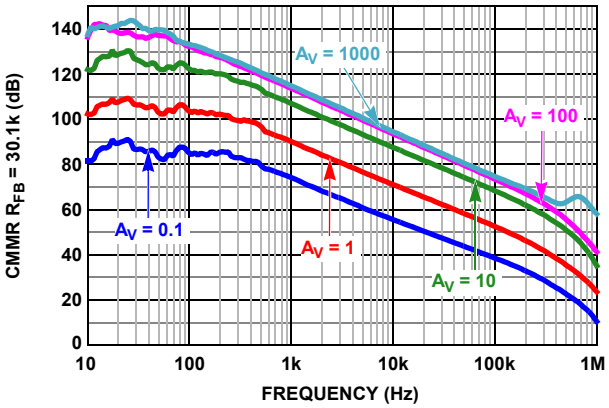


FIGURE 38. CMRR (RTI) R_F = 30.1k

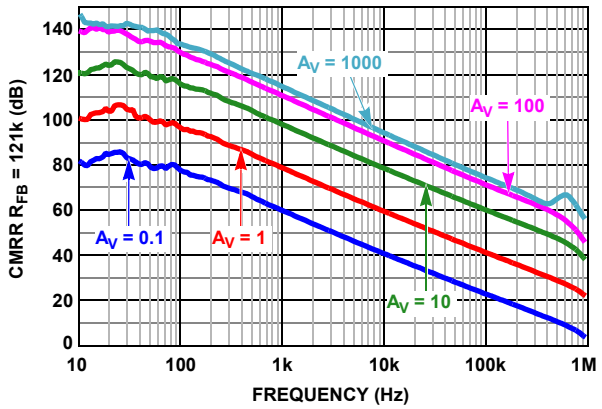


FIGURE 39. CMRR (RTI) R_F = 121k

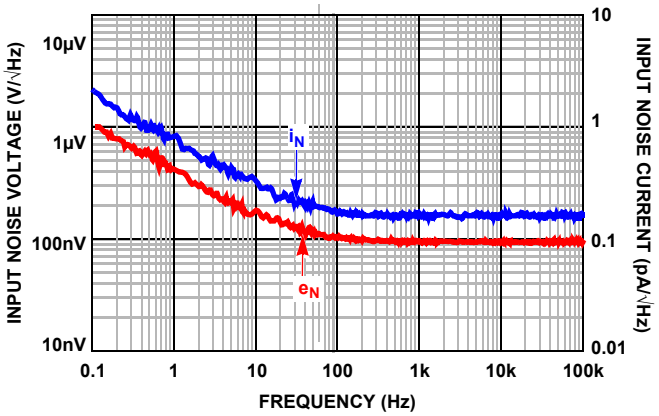


FIGURE 40. INPUT VOLTAGE AND CURRENT NOISE

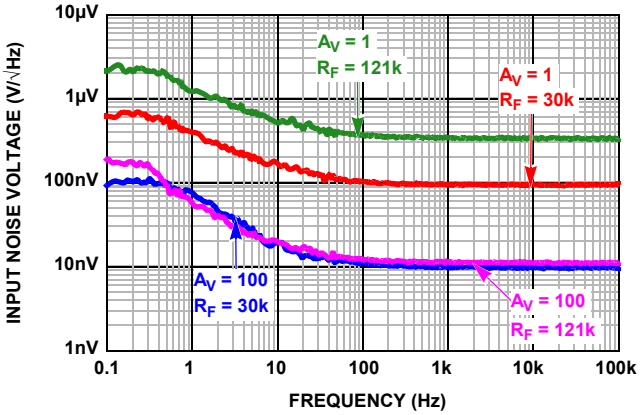


FIGURE 41. INPUT NOISE VOLTAGE vs GAIN AND R_F

Typical Performance Curves

$V_{CC} = V_{CO} = 18V$, $V_{EE} = V_{EO} = -18V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

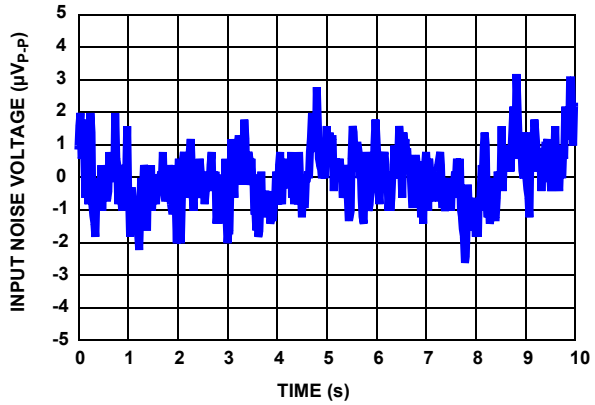


FIGURE 42. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz

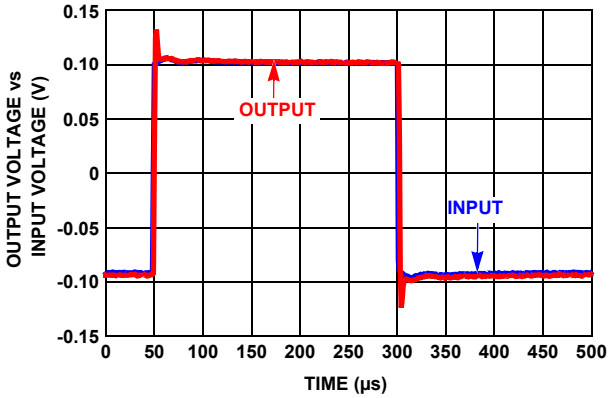


FIGURE 43. SMALL SIGNAL RESPONSE (A_V = 1, R_F = 30.1k)

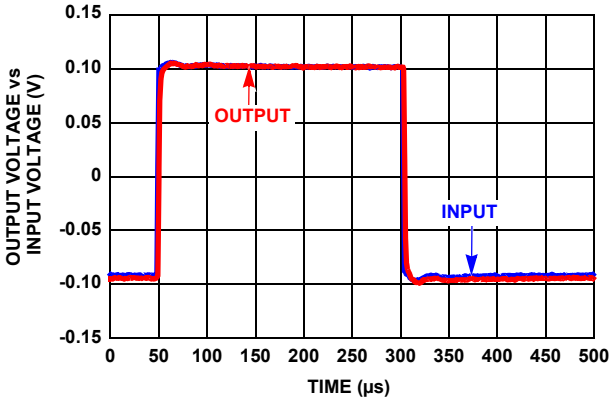


FIGURE 44. SMALL SIGNAL RESPONSE (A_V = 1, R_F = 121k)

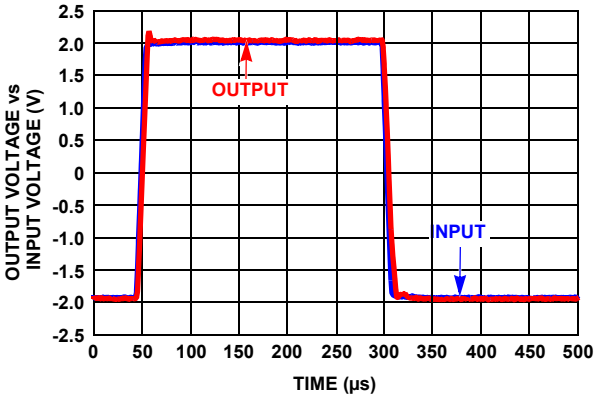


FIGURE 45. LARGE SIGNAL RESPONSE (A_V = 1, R_F = 30.1k)

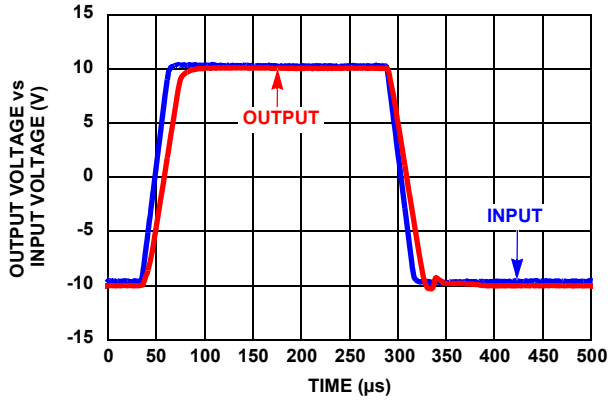


FIGURE 46. LARGE SIGNAL RESPONSE (A_V = 1, R_F = 121k)

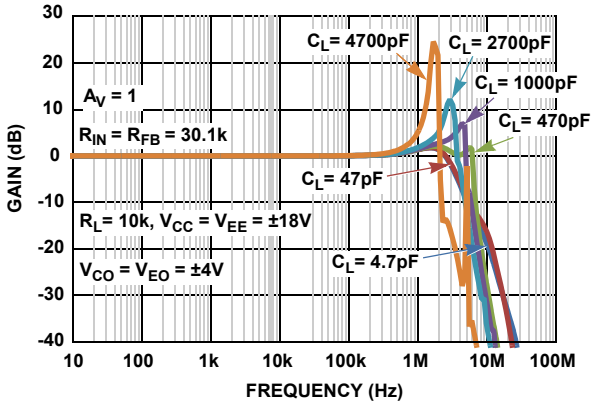


FIGURE 47. CLOSED LOOP GAIN vs FREQUENCY vs CL

Applications Information

"General Description" contains the ISL70617SEH functional and performance objectives and description of operation.

"Designing with the ISL70617SEH" on page 18 contains the application circuit design equations and guidelines for achieving the desired DC and AC performance levels.

"Estimating Amplifier DC and Noise Performance" on page 22 provides equations for predicting DC offset voltage and noise of the finished design.

General Description

The ISL70617SEH is an elaboration of the simpler current-feedback approach. The G_Ms are implemented with two external resistors and very high-gain amplifiers that impose input and feedback voltages upon them. The amplifiers have gains around ten million and linearize the transistors errors well below the 10ppm level. The overall gain is (R_{FB}/R_{IN}). With very high gain in the pseudo-G_Ms, the circuit adds little gain error and only R_{FB} and R_{IN} set gain to the 10ppm level. Thus, only the matching of the external resistors sets gain error and the cost of the resistors can be tailored to the accuracy needed. Note that the input stage is completely unaffected by output biasing, which is the right thing for an instrumentation amplifier.

The ISL70617SEH instrumentation amplifier was developed to accomplish the following:

- Provide a fully differential, rail-to-rail output for optimally driving ADCs. Maximum differential voltage set by R_{FB} (Equation 8 on page 18).
- Limit the output swing to prevent output overdrive
- Allow any gain, including attenuation
- Maximize gain accuracy by removing on-chip component tolerances and external PC board parasitic resistance
- Enable user control of amplifier precision level with choice of external resistor tolerance
- Maintain CMRR >100dB and remove CMRR sensitivity to gain resistor tolerance
- Provide a level-shift interface from bipolar analog input signal sources to unipolar and bipolar ADC output terminations

Functional Description

Figure 48 shows the functional block diagram for the ISL70617SEH.

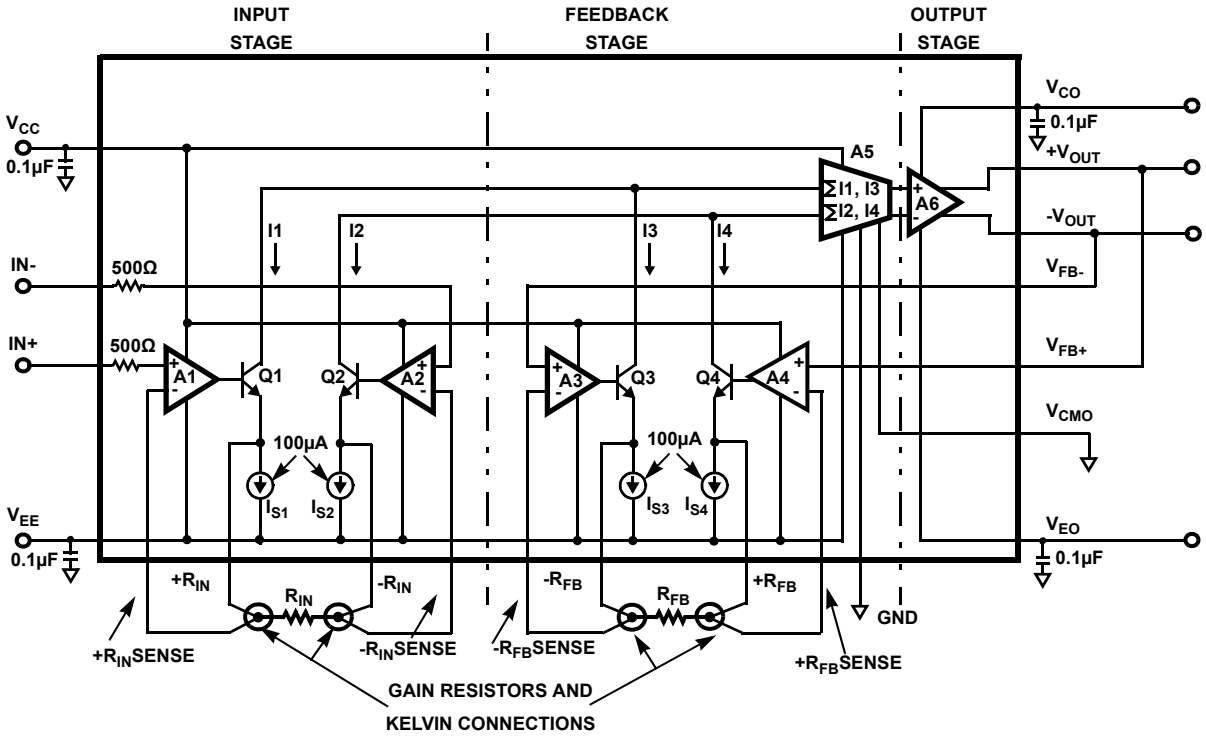


FIGURE 48. ISL70617SEH FUNCTIONAL BLOCK DIAGRAM

Input G_M Amplifier

The input stage consists of high performance, wideband amplifiers (A1, A2), G_M drive transistors (Q1, Q2) and input gain resistor (R_{IN}). Current drive for Q1 and Q2 emitters are provided by a matched pair of 100µA current sinks. A unity gain buffer from each input (IN+, IN-) to the terminals of the input resistor, R_{IN}, is formed by the connection of the Kelvin resistor sense pins and drive pins to the terminals of the input resistor, as shown in Figure 48. In this configuration, the voltage across the input resistor R_{IN} is equal to the input differential voltage across IN+ and IN-.

The input G_M stage operates by creating a current difference in the collector currents Q1 and Q2 in response to the voltage difference between the IN+ and IN- pins. When the input voltage applied to the IN+ and IN- pins is zero, the voltage across the terminals to the gain resistor R_{IN}, is also zero. Since there is no current flow through the gain resistor, the transistors Q1 and Q2 collector currents (I_1, I_2) are equal.

A change in the input differential voltage causes an equivalent voltage drop across the input gain resistor R_{IN}, and the resulting current flow through R_{IN} causes an imbalance in Q1, Q2 collector currents I_1, I_2, given by Equations 1 and 2:

$$I_1 = 100\mu A + (V_{IN+} - V_{IN-})/R_{IN} \quad \text{(EQ. 1)}$$

$$I_2 = 100\mu A - (V_{IN+} - V_{IN-})/R_{IN} \quad \text{(EQ. 2)}$$

Feedback G_M Amplifier

The feedback amplifiers A3, A4 form a differential transconductance amplifier identical to the input stage. The input terminals (V_{FB+}, V_{FB-}) connect to the ISL70617SEH differential output terminals ($+V_{OUT}$, $-V_{OUT}$) so that the output voltage also appears across the feedback gain resistor R_{FB}.

Operation is the same as the input G_M stage and the differential currents I_3, I_4 are given by Equations 3 and 4:

$$I_3 = 100\mu A - \{(+V_{OUT}) - (-V_{OUT})\}/R_{FB} \quad \text{(EQ. 3)}$$

$$I_4 = 100\mu A + \{(+V_{OUT}) - (-V_{OUT})\}/R_{FB} \quad \text{(EQ. 4)}$$

Error Amplifier A5, Output Amplifier A6

Amplifiers A5 and A6 act together to form a high-gain, differential I/O transimpedance amplifier. (Refer to Figure 48) Differential current amplifier A5 sums the differential currents (I_1+I_3, I_2+I_4) from the input and feedback G_M amplifiers. From that summation, a differential error voltage is sent to A6, which generates the rail-to-rail differential output drive to the $+V_{OUT}$ and $-V_{OUT}$ pins.

The external connection of the output pins to the feedback amplifier closes a servo loop where a change in the differential input voltage is converted into differential current imbalances at I_1, I_2 (Equations 1 and 2) at the summing node inputs to A5. Current I_1 sums with current I_3 from the feedback stage, and I_2 sums with I_4. A5 senses the difference between current pairs I_1, I_3 and I_2, I_4. A different voltage is generated, amplified and fed back to the feedback amplifier, which creates correction currents at I_3, I_4 to match the currents at I_1, I_2 (Equations 3 and 4).

Therefore, at equilibrium:

$$I_1 = I_3 \text{ and } I_2 = I_4 \quad \text{(EQ. 5)}$$

Combining Equations 1 and 3, (and their complements I_2 and I_4), and solving for V_{OUT} as a function of V_{IN}, R_{IN} and R_{FB}, yields Equation 6:

$$V_{OUT} = V_{IN} * R_{FB}/R_{IN} \quad \text{(EQ. 6)}$$

where $V_{OUT} = (+V_{OUT}) - (-V_{OUT})$ and V_{IN} = IN+ - IN-

Equation 6 can be rearranged to form the gain Equation 7:

$$\text{Gain} = V_{OUT}/V_{IN} = R_{FB}/R_{IN} \quad \text{(EQ. 7)}$$

This is a general form of the gain equation for the ISL70617SEH.

Designing with the ISL70617SEH

To complete a working design, the following procedure is recommended and explained in this section:

1. Define the output differential voltage swing
2. Set the feedback resistor value, R_{FB} (Equation 8)
3. Set the input gain resistor value, R_{IN}
4. Set the V_{CO} and V_{EO} power supply voltages
5. Set the V_{CC} and V_{EE} supply voltages

The gain of the instrumentation amplifier is set by the resistor ratio R_{FB}/R_{IN} (Equation 7), and the maximum output swing is set by the absolute value of the feedback resistor R_{FB} (Equation 8). V_{CO} and V_{EO} supply power to the rail-to-rail output stage and define the maximum output voltage swing at the $\pm V_{OUT}$ differential output pins. Power supply pins V_{CC} and V_{EE} power the feedback amplifiers, which require an additional ±3V beyond the V_{CO} and V_{EO} voltages to maintain linear operation of the feedback G_M stage.

Setting the Feedback Gain Resistor (R_{FB})

Resistor R_{FB} defines the maximum differential voltage at output terminals $+V_{OUT}$ to $-V_{OUT}$ (Refer to Figures 48 and 49). External resistor R_{FB} and the differential 100µA current sources define the maximum dynamic range of the feedback stage, which defines the maximum differential output swing of the output stage. Overload circuitry allows >100µA to flow through R_{FB} to maintain feedback, but linearity is degraded. Therefore, it is a good practice to keep the maximum linear dynamic range to within ±80% of the maximum I*R across the resistor.

$$V_{OUT}DIFF = \pm 80\mu A * R_{FB} \quad \text{(EQ. 8)}$$

In cases where large pulse overshoot is expected, the maximum current in Equation 8 could be reduced to 50% for additional margin (see "AC Performance Considerations" on page 20). The penalty for increasing the feedback resistor value is higher DC offset voltage and noise.

Output voltages that exceed the maximum dynamic range of the feedback amplifier can degrade phase margin and cause instability. The plot in Figure 49 shows the maximum differential output voltage swing vs resistor value for R_{FB} and R_{IN} using the 80% and 50% current source levels.

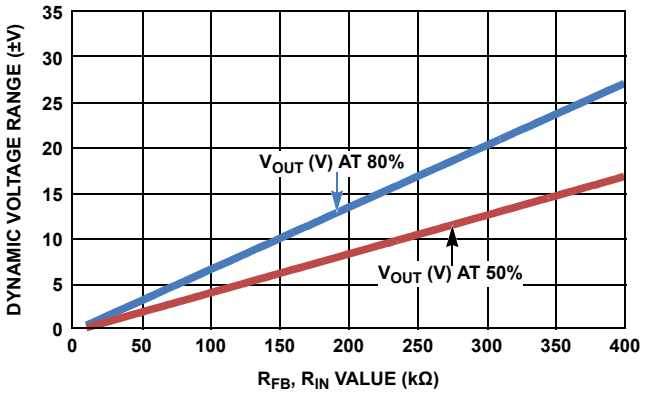


FIGURE 49. R_{FB}, R_{IN} vs DYNAMIC RANGE

Setting the Input Gain Resistor (R_{IN})

The input gain resistor (R_{IN}) is scaled to the feedback resistor according to the gain in Equation 9:

$$R_{IN} = R_{FB}/Gain \quad \text{(EQ. 9)}$$

The input G_M stage uses the same differential current source arrangement as the feedback stage. Therefore, the amount of overdrive margin (50%, 80%) included in the calculation for R_{FB} is also included in the calculation for R_{IN} (Refer to Figures 48 and 49).

Input Stage Overdrive Considerations

There are a few cases where the input stage can be overdriven, which must be considered in the application. An input signal that exceeds the maximum dynamic range of the gain resistor R_{IN}, calculated previously, can cause the ESD diodes to conduct. When this occurs, a low impedance path from the inputs to the input gain resistor R_{IN} will result in signal distortion (Refer to Figure 50).

High-speed input signals that remain within the maximum dynamic range of the input stage can cause distortion if the input slew rate exceeds the input stage slew rate (~4V/µs). When the input slews at a faster rate than the G_M stage can follow, the voltage difference appears across the input ESD diodes from each input and resistor R_{IN}. When the voltage difference is large enough to cause the diodes to conduct, the input terminals are shunted to R_{IN} through the 500Ω input protection resistors, causing distortion during the rise and fall times of the transient pulse. The distortion will last until the resistor voltage catches up to the input voltage.

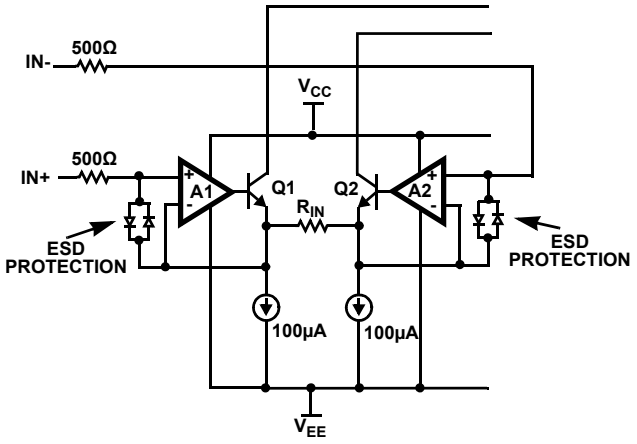


FIGURE 50. INPUT STAGE ESD PROTECTION DIODES

Setting the Power Supply Voltages

The ISL70617SEH power supplies are partitioned so that the input stage and feedback stages are powered from a separate pair of supply pins (V_{CC}, V_{EE}) than the differential output stage (V_{CO}, V_{EO}). This partitioning provides the user with the ability to adapt the ISL70617SEH to a wide variety of input signal power sources that would not be possible if the supplies were strapped together internally ($V_{CC} = V_{CO}$ and $V_{EE} = V_{EO}$). However, powering the input and output supplies from unequal supplies has restrictions that are described in the next section.

Powering the Input and Feedback Stages (V_{CC}, V_{EE})

The input pins IN+, IN- cannot swing rail-to-rail, but have a maximum input voltage range given by Equation 10:

$$V_{EE} + 3V \le (V_{CMIR}IN + V_{IN}) \le V_{CC} - 3V; \quad \text{(EQ. 10)}$$

where V_{IN} = maximum differential voltage IN+ to IN-

This requires the sum of the common-mode input voltage and the differential input voltage to remain within 3V of either the V_{CC} or V_{EE} rail, otherwise distortion will result.

The feedback pins V_{FB}+ and V_{FB}- have the same input common-mode voltage constraint as the input pins IN+, IN-. The maximum input voltage range of the feedback pins is given by Equation 11:

$$V_{EE} + 3V \le V_{CMIR}FB \le V_{CC} - 3V \quad \text{(EQ. 11)}$$

where $V_{CMIR}FB = (+V_{OUT} - -V_{OUT}) + V_{CMO}$

To maintain stability, it is critical to respect the ±3V requirement in Equation 11.

Powering the Rail-to-Rail Output Stage (V_{CO}, V_{EO})

The output stage (A6) is a rail-to-rail design, and is powered by the V_{CO} and V_{EO} pins. The differential output pins $+V_{OUT}$, $-V_{OUT}$ connect to the $+V_{FB}$, $-V_{FB}$ pins to close the output feedback loop. The feedback stage is powered from the V_{CC} and V_{EE} pins. The $+V_{FB}$, $-V_{FB}$ have a common-mode input range 3V below the V_{CC} rail and 3V above the V_{EE} rail. If the output voltage exceeds the

feedback common-mode input voltage, loop instability will result. Therefore, the voltages at the $\pm V_{OUT}$ pins should always be 3V away from either rail, as shown in Equation 12.

$$V_{EE} + 3V \leq V_{OUT} \leq V_{CC} - 3V; \quad \text{(EQ. 12)}$$

where $V_{OUT} = |+V_{OUT}|$ or $|-V_{OUT}|$

Rail-to-Rail Differential ADC Driver

The differential output stage of the ISL70617SEH is designed to drive the differential input stage of an ADC. In this configuration, the V_{CO}, V_{EO} power supply pins connect directly to the ADC power supply pins. This output swing arrangement is ideal for driving the rail-to-rail ADC drive without the possibility of overdriving the ADC input.

The output stage is capable of rail-to-rail operation when V_{CO}, V_{EO} are powered from a single supply or from split supplies. It has a single supply voltage range (V_{CO}) from 3V to 15V (with V_{EO} at GND), and a ±1.5V to ±15V split supply voltage range. Under all power supply conditions, V_{CC} must be greater than V_{CO} by 3V, and V_{EE} must be less than V_{EO} by 3V to maintain the rail-to-rail output drive capability.

The V_{CMO} pin is an input to a very low bias current terminal and sets the output common-mode reference voltage when driving a differential input ADC, such that the output would have a ± input signal span centered around an external DC reference voltage applied to the V_{CMO} pin.

Power Supply Voltages by Application

The ISL70617SEH can be adapted to a wide variety of instrumentation amplifier applications where the signal source is powered from supply voltages that are different from the supply voltages powering downstream circuits. The following examples are included as a guide to the proper connection and voltages applied to the supply pins V_{CC}, V_{EE}, V_{CO}, and V_{EO}.

There are a common set of requirements across all power applications:

1. A common ground connection from the input supplies, (V_{CC}, V_{EE}) to the output supplies (V_{CO}, V_{EO}) is required for all powering options.
2. The signal input pins (IN+, IN-) cannot float and must have a DC return path to ground.
3. The input and output supplies cannot both be operated in single supply mode due to the 3V feedback amplifier common-mode headroom requirement in Equation 11.

The following are typical power examples:

EXAMPLE 1: BIPOLAR INPUT TO SINGLE SUPPLY OUTPUT

The ISL70617SEH is configured as a 5V ADC driver in a high-gain sensor bridge amplifier powered from a ±10V excitation source. In this application, the ISL70617SEH must extract the low-level bipolar sensor signal and shift the level to the 0V to +5V differential rail-to-rail signal needed by the ADC. The following powering option is recommended:

- V_{CC} = +10V, V_{EE} = -10V
- V_{CO} = +5V, V_{EO} = GND
- V_{CMO} = +2.5V
- V_{CC}, V_{EE} power supply common connects to GND

EXAMPLE 2: HIGH VOLTAGE BIPOLAR I/O BUFFER

The ISL70617SEH is configured as a high impedance buffer instrumentation amplifier in a ±15V industrial sensor application. In this application, the ISL70617SEH must extract and amplify the high impedance sensor signal and send it downstream to a differential ADC operating from ±15V supplies. The following powering options are recommended:

1. Input and output supplies are strapped to the same supplies and rail-to-rail input to the ADC is not required.
   - $V_{CC} = V_{CO}$ = +15V
   - $V_{EE} = V_{EO}$ = -15V
   - V_{CMO} = GND
   - V_{CC}, V_{EE} power supply common connects to GND and V_{OUT} = ±12V
2. ±15V rail-to-rail output is required, then:
   - V_{CC} = +18V, V_{EE} = -18V
   - V_{CO} = +15V, V_{EO} = -15V
   - V_{CMO} = GND
   - V_{CC}, V_{EE} power supply common connects to GND

The V_{CO} and V_{EO} power supply pins connect to the ADC ±15V power supply pins. Rail-to-rail output swing requires that $V_{CC} = V_{CO}$ +3V and $V_{EE} = V_{EO}$ -3V, or ±18V.

EXAMPLE 3: GAINS LESS THAN 1

The ISL70617SEH is configured to a gain of 0.2V/V driving a rail-to-rail 3V ADC. In this application, the maximum input dynamic range is ±15V.

- V_{CC} = +18V, V_{EE} = -18V
- V_{CO} = +3V, V_{EO} = GND
- V_{CMO} = +1.5V
- V_{CC}, V_{EE} power supply common connects to GND

In this attenuator configuration, the input signal range is ±15V, which requires an additional ±3V of input overhead from the input supplies. Thus, V_{CC} and V_{EE} = ±18V.

AC Performance Considerations

The ISL70617SEH closed loop frequency response is formed by the feedback G_M amplifier and gain resistor R_{FB} and has the characteristics of a current feedback amplifier. Therefore, the -3dB gain does not significantly decrease at high gains as is the case with the constant gain-bandwidth response of the classic voltage feedback amplifier.

There are four behaviors of current feedback amplifiers that must be considered:

1. Frequency response increases with decreasing values of R_{FB}. A comparison of the G = 100, -3db response (Figures 28 and 29) R_{FB} at 30.1kΩ vs 121kΩ shows almost a 4X decrease from 2MHz to 0.5MHz.
2. Gain peaking tends to increase with decreasing values of R_{FB}
3. Wideband applications at gains less than 1 (Figures 28 and 29) can have high gain peaking resulting in high levels of overshoot with pulsed input signals
4. Parasitic capacitance at the feedback resistor terminals ($+R_{FB}$, $-R_{FB}$) and the Kelvin sense terminals ($+R_{FB}$SENSE, $-R_{FB}$SENSE) will result in increasing levels of peaking and transient response overshoot.

To minimize peaking, external PC parasitic capacitance should be minimized as much as possible. The ISL70617SEH is designed to be stable with PC board parasitic capacitance up to 20pF and feedback resistor values down to 30.1kΩ. At gains less than 1, the maximum parasitic capacitance may have to be limited further to avoid additional compensation.

Uncorrected gain peaking and high overshoot in the feedback stage can cause loss of feedback loop stability if the transient causes the feedback voltage to exceed the common-mode input range of the feedback amplifier or the maximum linear range of the feedback resistor R_{FB}. Corrective actions include increasing the size of the feedback resistor (see Figure 49 on page 19) and rescaling the input gain resistor R_{IN}, or adding input frequency compensation described in the next section.

The penalty of increasing the R_{FB} (and R_{IN} rescaling) is increased noise, so this is generally not the corrective action of choice.

AC Compensation Techniques

Input compensation with a low pass filter (Figure 51) can be an effective way to block high frequency signals from the differential amplifier inputs. It does not change the gain peaking behavior of the feedback loop, but it does block signals from creating overdrive instability. This method is useful after other corrective measures have been implemented, and when there is little control over the input signal frequency content.

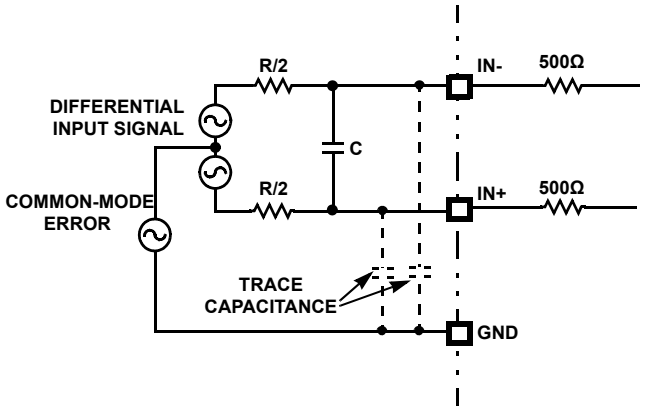


FIGURE 51. INPUT DIFFERENTIAL LOW PASS FILTER AND PARASITIC CAPACITANCE

Input Common-Mode Rejection Considerations

The ISL70617SEH is capable of a very high level (110dB) of CMRR performance from DC to as high as 1kHz for gains greater than 100, (see Figures 38 and 39 on page 15). This high level of performance over frequency is made possible by the high common-mode input impedance (80GΩ) but requires careful attention to the matching of the IN+ and IN- external impedances to GND.

A mismatch in the series impedance in conjunction with parasitic capacitance at the IN+, IN- terminals (Figure 51) will cause a common-mode amplitude imbalance that will show up as a differential input signal, rapidly degrading CMRR as the common-mode frequency increases.

Maximum CMRR performance is achieved with attention to balancing external components and attention to PC layout.

Layout Guidelines

The ISL70617SEH is a high precision device with wideband AC performance. Maximizing DC precision requires attention to the layout of the gain resistors. Achieving good AC response requires attention to parasitic capacitance at the gain resistor terminals. CMRR performance over frequency is ensured with symmetrical component placement and layout of the input differential signals to the IN+ and IN- terminals.

To ensure the highest DC precision, the location of the gain resistors and PC trace connections to the Kelvin connections are most important. Proper Kelvin connections remove trace resistance errors so that the amplifier gain accuracy and gain temperature coefficients are determined by the gain resistor matching tolerance. Interconnect constraints preclude mounting the gain resistors next to each other, so they should be located on either side of the ISL70617SEH and as close to the device as possible. The Kelvin connections are formed at the junction of the sense pins ($\pm R_{IN}$SENSE, $\pm R_{FB}$SENSE) and the gain resistor current drive terminals ($\pm R_{IN}$, $\pm R_{FB}$). This junction should be made at the terminal pads directly under the ends of each resistor.

Reduced trace lengths that maintain DC accuracy are also important for minimizing the capacitance that can degrade AC stability. This is especially true at gains less than one.

Layout guidelines for high CMRR include matching trace lengths and symmetrical component placement on the circuit that connects the signal source to the IN+, IN- pins. This ensures matching of the IN+ and IN- input impedances (Figure 51).

Power Supply Decoupling

Standard power supply decoupling consists of a single 0.1µF 50V ceramic capacitor at the power supply terminals located as close to the device as possible. In applications where the input and output supplies are strapped to the same voltage ($V_{EE} = V_{EO}$, $V_{CC} = V_{CO}$), the connection point should be as close to the device as possible with a single 0.1µF 50V ceramic capacitor at the junction. Applications using separate supplies require 0.1µF 50V ceramic decoupling capacitors at each power supply terminal.

Estimating Amplifier DC and Noise Performance

The gain resistor ohmic values and ratios are all that is required to estimate DC offset and noise. The following sections illustrate methods to calculate DC offset and noise performance. These estimates are useful for optimizing resistor values for noise and DC offset.

Calculating DC Offset Voltage

Output offset voltage, like output noise, has several contributors. Also similar to output noise, the major offset contributor depends on the gain configuration. In high-gain, $V_{OS(I)}$ dominates, while in low-gain, offset due to I_{ERR} dominates.

The summation of DC offsets to arrive at a total DC offset error is performed in two ways. Equation 13 is a simple addition of the DC offsets appearing at the output, and is useful when defining the minimum to maximum range of offset that can be expected. The drawback is that the result defines the corner of the corners of the error box, and is not a typical value given that these sources are uncorrelated.

$$V_{OS}(RTO) = [(A_V \times V_{OS(IN)}) + (V_{OS(FB)}) + (I_{ERR} \times R_{FB})] \quad \text{(EQ. 13)}$$

Equation 14 expresses the total DC error as the RMS, or square root of the sum of the squares to provide an estimate of a typical value.

$$V_{OS}(RTO)TYP = \sqrt{[(A_V \times V_{OS(IN)})^2 + (V_{OS(FB)})^2 + (I_{ERR} \times R_{FB})^2]} \quad \text{(EQ. 14)}$$

Equation 15 converts the output offset error (Equation 13) range to an input referred error range [V_{OS}(RTI)] and enables a comparison with the DC component of the input signal.

$$V_{OS}(RTI) = [(V_{OS(IN)}) + (V_{OS(FB)}/A_V) + (I_{ERR} \times R_{FB})/A_V] \quad \text{(EQ. 15)}$$

Similarly, Equation 16 shows the typical DC offset value (Equation 14) referred to the input.

$$V_{OS}(RTI)TYP = \sqrt{[V_{OS(IN)})^2 + (V_{OS(FB)}/A_V)^2 + (I_{ERR} \times R_{FB})/A_V)^2]} \quad \text{(EQ. 16)}$$

These results are summarized in Table 2.

Calculating Noise Voltage

The calculation of noise spectral density at the output [e_N(RTO)] from all noise sources is given by Equation 17.

$$e_N(RTO) = \sqrt{[(A_V \times e_N(I))^2 + (2 \times A_V \times i_N(I) \times 500\Omega)^2 + (A_V)^2 \times (4kT \times R_{IN}) + (4kT \times R_{FB}) + (R_{FB} \times i_N(IERR))^2 + (e_N(FB))^2]} \quad \text{(EQ. 17)}$$

Equation 18 converts the output noise to the input referred value when evaluating the input signal-to-noise ratio.

$$e_N(RTI) = e_N(RTO)/A_V \quad \text{(EQ. 18)}$$

Table 3 on page 23 provides examples of the noise contribution of each source by circuit gain and output voltage span.

In a high-gain configuration, the input noise is the dominant noise source. In a low-gain configuration, the noise voltage from the product of the internal noise current, $I_{N(err)}$, and the feedback resistor, R_{FB}, dominates. The contribution of the internal noise current, $I_{N(err)}$, increases in proportion to R_{FB}, but the corresponding increase in output voltage with R_{FB} keeps the ratio of this noise voltage to output voltage constant.

TABLE 2. COMPUTING TYPICAL OUTPUT OFFSET VOLTAGE RANGES

A_V	$V_{O(LIN)}$	R_{IN} (kΩ)	R_f (kΩ)	A_V x V_{OS}(I) (µV) (Note 16)	V_{OS}(FB) (µV) (Note 16)	I_{ERR} (5nA) x R_{FB} (µV) (Note 16)	V_{OS}(RTO) (µV) (Equation 13)	V_{OS}(RTI) (µV) (Equation 15)	TYPICAL V_{OS}(RTO) (µV) (Equation 14)	TYPICAL V_{OS}(RTI) (µV) (Equation 16)
1	±2.5	30.1	30.1	±30	±400	±150	±580		428	
1	±10	121	121	±30	±400	±600	±1030		722	
100	±2.5	0.301	301	±3000	±400	±150	±3550	±3005	3030	3000
100	±10	1.21	121	±3000	±400	±600	±4000	±3010	3085	3000

NOTE:

16. Chosen for illustration purposes and does not reflect actual device performance.

TABLE 3. 1kHz INPUT NOISE AND THERMAL NOISE CONTRIBUTIONS

A_V	R_{IN} (kΩ)	R_{FB} (kΩ)	A_V x $e_N(I)$ (nV/√Hz)	2 x A_V x $i_{N(I)}$ x 500Ω (nV/√Hz)	A_V x √(4kT x R_{IN}) (nV/√Hz)	√(4kT x R_{FB}) (nV/√Hz)	R_{FB} x $i_N(I_{ERR})$ (nV/√Hz)	e_N(FB) (nV/√Hz)	e_N (RTO) OUTPUT REFERRED NOISE (nV/√Hz)	e_N (RTI) INPUT REFERRED NOISE (nV/√Hz)
1	30.1	30.1	8.6	0.15	22.3	22.3	78	8.6	86	
1	121	121	8.6	0.15	44.6	44.6	300	8.6	307	
100	0.301	301	860	15	223	22.3	78	8.6	896	8.9
100	1.21	121	860	15	446	44.6	300	8.6	1015	10.15

NOTE:

17. e_N and i_N values are chosen for illustration purposes and may not reflect actual device performance.

Driving an ADC

The output feedback loop is closed by the connection of $+V_{OUT}$ to the $+V_{FB}$ pin and $-V_{OUT}$ to the $-V_{FB}$. The V_{CMO} pin is just an input to a very low bias current terminal, and would be connected to a mid-scale voltage when driving a single supply ADC, such that the input would have a ± input signal span. Where V_{CMO} is connected to the ADC ground, only positive inputs would be converted by the ADC.

Input and Feedback Amplifiers

The input and the output linear dynamic ranges are set by class-A biasing on the R_{IN} resistor for the input stage, and the R_{FB} resistor for the output stage (Figure 48). Unity gain buffers force the differential voltages across each resistor to the maximum of 100µA*R produced by the current sources. While the voltages impressed across these resistors will continue to move with overloads beyond this value, they will not be linear. A good rule of thumb is to keep the maximum linear dynamic range to less than ~80% of the maximum I*R voltage across the resistors (Equation 8).

At equilibrium, the amplifier forces the resistor currents to be the same so that their voltages match the desired gain ratio, R_{FB}/R_{IN}; however, during transient conditions, the currents remain unequal until the amplifier output settles. For this reason, the current sources driving the feedback resistor are 20% higher than those driving the input G_M resistor to provide an extra margin.

Rail-to-rail Output Stage

The output stage is of rail-to-rail design, and has separate supplies from the rest of the IC. The input GM stage and feedback amplifiers are driven from the V_{CC} and V_{EE} supply pins and only the output stage is powered by the V_{CO} and V_{EO} pins. A typical supply arrangement when driving a 5V ADC is to have V_{CO} connected to the ADC +5V supply and V_{EO} to ground. Therefore, the ADC can never be overdriven beyond its supply rails. In this configuration, the common-mode input range of the feedback amplifier limits the dynamic range of the output stage. The input and feedback amplifiers are not rail-to-rail, so the V_{CC} must be more positive than V_{CO} and V_{EE} more negative than V_{EO} by the feedback amplifier saturation voltage (±3V).

DC Offsets and Noise

There are three offset and noise sources in the ISL70617SEH: the input, feedback, and I_{ERR}. The input has a low input noise voltage and offset, which dominates at gains ~30 and above. The feedback G_M stage has similar errors, but is never dominant compared to I_{ERR} and is generally ignored. I_{ERR} can be thought of as the mistracking and noise of the internal 100µA current sources. Use Equation 19 and quantify these errors at the output (RTO).

$$V_{OS}(RTO) = V_{OS}(IN)*Gain + I_{ERR}*R_{FB+}V_{OS}(FB) \quad \text{(EQ. 19)}$$

Similarly, Equation 20 for noise:

$$V_N(RTO)^2 = (V_N(IN)*Gain)^2 + (I_n(err)*R_{FB})^2 \quad \text{(EQ. 20)}$$

Reducing R_{FB} to the minimum value required for linear output swing will improve output offsets and noise directly.

Another result of scaling R_{FB} is that the -3dB bandwidth is also inversely scaled. Highest bandwidth will then be available at lowest R_f. The ISL70617SEH is designed to be stable with R_{FB} = 30.1kΩ minimum.

Having set R_{FB} to establish the output range, R_{IN} is set to establish Gain = R_{FB}/R_{IN}. While -3dB bandwidth does diminish for R_{IN} < 500Ω, this still allows fairly constant bandwidth over a wide variety of gains. Similar to the resistor-oriented op amp topology, parasitic capacitance at the R_{FB} node will peak the frequency response. The ISL70617SEH is designed to be tolerant to parasitic capacitances at R_{FB} from values of 2pF to 20pF. The input stage is more tolerant, allowing 2pF to 30pF. Electronic analog switches can be used to alter R_{IN} selections for gain switching, as long as the minimum R_{FB} halves are connected to the R_{IN} pins directly, with the switch(es) in between the halves.

The following switch example (Figure 52) is a practical way to isolate switch parasitic capacitances from the R_{IN} pins:

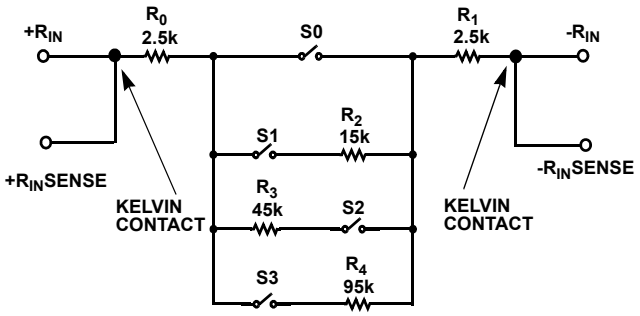


FIGURE 52. SWITCH EXAMPLE

The R_{FB} and R_{IN} resistors are provided with Kelvin sense pins to minimize interconnect resistance errors. This is especially useful at high gains and small R_{IN}.

Amplifier Usage Examples

The external resistors, R_{FB} and R_{IN}, set both the voltage gain and the linear output voltage range. The linear output voltage range is the maximum differential signal that can appear at the output, and is different from the common-mode range. The voltage gain is shown in Equation 21.

$$A_V = (R_{FB}/R_{IN}) \quad \text{(EQ. 21)}$$

Linear output voltage range is shown in Equation 22.

$$V_{O(LIN)} = \pm(R_{FB} \times I_{RIN}) \quad \text{(EQ. 22)}$$

where I_{RFB} is nominally set to 80% of I_{RIN}.

For example, an application requiring a voltage gain of 100 and a linear output range of ±2.5V might select a 30kΩ feedback resistor and a 300Ω input resistor to ensure linear operation throughout the required output span. The output offset voltage (Table 2 on page 22) shows a few standard gain configurations and linear output spans with appropriately sized resistors.

Package Characteristics

Weight of Packaged Device

1.33 grams (Typical)

Lid Characteristics

Finish: Gold
Potential: Connected to Pin #8 (GND)
Case Isolation to Any Lead: 20 x 10^9 Ω (minimum)

Die Characteristics

Die Dimensions

2960µm x 3210µm (117 mils x 127 mils)
Thickness: 483µm ±25µm (19 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: Silicon Nitride
Thickness: 15kÅ

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 30kÅ

BACKSIDE FINISH

Silicon

Assembly Related Information

SUBSTRATE POTENTIAL

Floating

Additional Information

WORST CASE CURRENT DENSITY

<2 x 10^5 A/cm^2

PROCESS

Dielectrically Isolated Advanced Bipolar Technology- PR40

Metalization Mask Layout

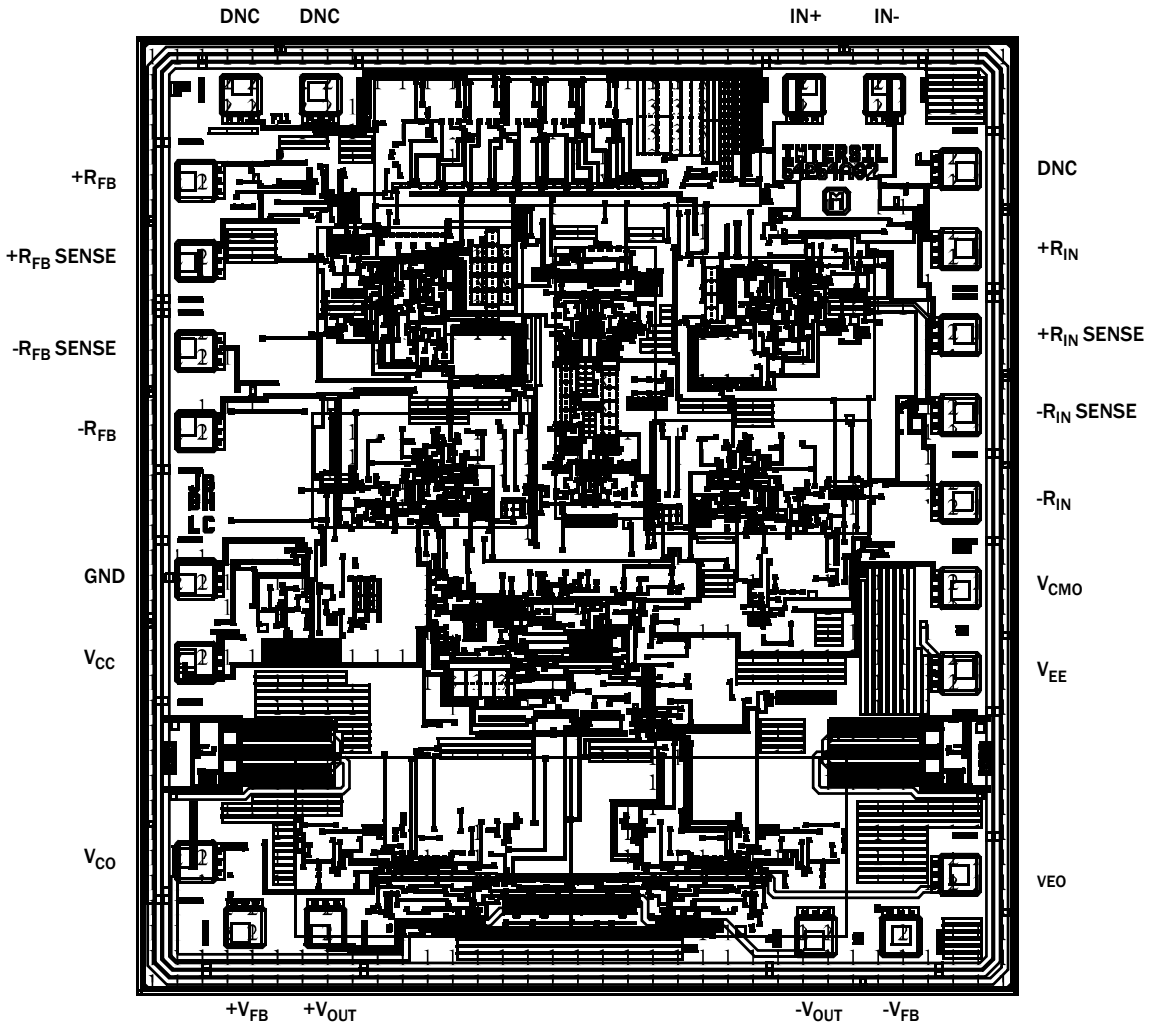


TABLE 4. DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	BOND WIRES PER PAD (Note 19)
NC	1			
DNC	2			
DNC	3			
$+R_{FB}$	4	1	1292	1
$+R_{FB}$ SENSE	5	1	1032	1
$-R_{FB}$ SENSE	6	1	738.5	1
$-R_{FB}$	7	1	478.5	1
GND	8	0	0	1
V_{CC}	9	0	-273	1
V_{CO}	10	1	-918.5	1
$+V_{FB}$	11	158.5	-1131.5	1
$+V_{OUT}$	12	421.5	-1131.5	1
$-V_{OUT}$	13	2012.5	1160.5	
$-V_{FB}$	14	2288.5	-1160.5	1
V_{EO}	15	2479.5	-960.5	1
V_{EE}	16	2479.5	-307.5	1
V_{CMO}	17	2479.5	-31.5	
$-R_{IN}$	18	2479.5	246.5	1
$-R_{IN}$ SENSE	19	2479.5	530	1
$+R_{IN}$ SENSE	20	2479.5	790	1
$+R_{IN}$	21	2479.5	1069	1
DNC	22			
IN-	23	2235.5	1569.5	1
IN+	24	1975.5	1569.5	1

NOTES:

18. Origin of coordinates is the centroid of GND.
19. Bond wire size is 1.25 mil (Al).

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
December 16, 2016	FN8697.4	Updated Related Literature section. Added Note 15 and applicable cross-references.
July 5, 2016	FN8697.3	Boldface limits condition in “Electrical Specifications” on page 5 changed from “...or across” to “...and across” and updated bolding of applicable specs.
April 28, 2016	FN8697.2	“Absolute Maximum Ratings” on page 5 - Changed CDM testing information from JESD22-C101F to JS-002-2014. “V_{OS}FB” on page 5 - Updated Test Conditions by adding Temp ranges and adding Post 75krad conditions and limits. “V_{OS}OUT” on page 7 - bolded MAX spec. Equations 13 through 16 updated VOS(I) to VOS (IN) Table 2 on page 22 Changed values in AV x Vos (I), Vos(RTO), Vos(RTI) and Typical Vos(RTO), Typical Vos(RTI).
January 7, 2016	FN8697.1	Added Figure 47 on page 16. Updated Figure 48 on page 17. Added reference to Equation 8 under “Designing with the ISL70617SEH” on page 18 item #2.
November 23, 2015	FN8697.0	Initial release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

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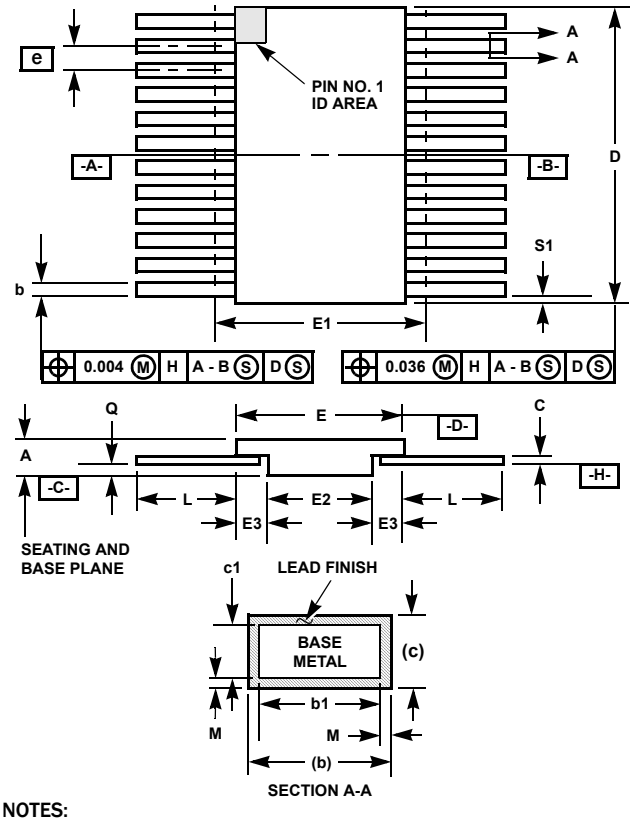
Ceramic Metal Seal Flatpack Packages (Flatpack)



K24.A MIL-STD-1835 CDFP4-F24 (F-6A, CONFIGURATION B)
24 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.640	-	16.26	3
E	0.350	0.420	9.14	10.67	-
E1	-	0.450	-	11.43	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	24		24		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.